Apple Scanner: How Its Internal Circuitry Works

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- Scanner circuitry

A scan is initiated when the microprocessor, inside the Apple Scanner, signals the carrier arm assembly electronics. At this point, the carrier arm, containing both the fluorescent lamp and CCD sensors, begins the scan. The scan proceeds line-by-line until the entire document is scanned. The reflected light from the scan is detected by the CCD sensors which are arranged in three rows of 2592 individual sensors. Each sensor in the first row holds one picture element (PEL), or pixel, of a scan line. The elements in rows 2 and 3 are used as data buffers prior to being sent to the image processing logic.

As the carrier arm assembly passes under the original document, the first row of CCD sensors capture the image reflection from the fluorescent light. The sensors produce analog signals that represent the original as tiny dots, or pixels, that make up a bit image. To manipulate and correct the various image distortions that can result form interference, the analog signal outputs from the CCD sensors are sent to the image-processing logic for conversion to digital signals.

The converted digital signals are sent either directly from the image-processing logic to the scanner main memory for transmission to the host computer; or, if the resolution is less the 300 dpi, the signals are sent through the line memory, PEL correction memory for transmission to the host. Data transfer from main memory to the host computer is done under control of the DMAC through the SCSI cable.

- Image-sensing circuitry

The components of the image-sensing logic include the CCD sensors and the analog circuitry which together are responsible for sensing, filtering, and amplifying the bit image of the scanned original. As the original is scanned, the CCD circuitry senses the image reflected by the fluorescent light. The three CCD sensors are used to support one line of pixels. The second and third rows of sensors are primarily used to buffer the image data. The reflected light from each pixel charges the front-row of CCD sensors. The charged front row of sensors then shifts their contents to the second row of sensors which in turn shifts their contents to the third row of sensors. The third row of sensors are then serially shifts out, one element at a time, for clean-up and

amplification. The signals from the amplifier, are then sent through a low pass filter and attenuator to the image processor where the signals are distortion corrected and converted from analog-to-digital.

- Flow of the CCD-sensing process

Also included in the image-sensing logic is the black-level reference voltage and auto background-adjustment circuitry. The black-level reference voltage determines the threshold value for the black level of the pixels; that is, will be represented as a black dot or white dot in the overall image. This part of the circuitry is driven by the seven signals (VBLO-6), from the microprocessor. The auto background-adjustment circuitry receives digitized signals from the image-processing logic to integrate the amplified CCD outputs as the background level. The integrated signals serve as the background level of the original and change dynamically during the scan.

- Image-processing logic

After the image has been scanned, the analog signals from the CCD elements are sent through the image-processing logic. The image-processing logic is responsible for processing the scanned image and contains the major portion of the scanner logic. The major components of the image processing logic are:

- DIPP (document-image pre-processor)
- Gate array 1
- Line memory and PEL correction memory
- Gate array 2

Most of the actual processing is done by the DIPP. The gate arrays, line memory, and PEL correction memory are support logic for the DIPP functions.

The DIPP is an image-signal processor which takes the analog image data from the CCD elements and corrects any distortion of the data, digitizes the corrected data, and transfers the digital data to main memory. These steps are accomplished with the support of the gate arrays.

In Line Art and Halftone composition scans, the DIPP passes the digitized signals to line memory for horizontal-resolution conversion for the selected resolution level.

The output from the DIPP differs depending upon the composition of the scan. When the scanner uses Line Art or Halftone composition, the output from the DIPP is 1 bit for every pixel. However, when the scanner uses Grayscale composition, the output is 4 bits per pixel. The additional bits enable the scanner software to create a more accurate representation of the individual dots within the image. On the Macintosh II, the 4 bits drive the grayscale monitor or the color monitor.

The DIPP uses gate array 1 to support reduction options by controlling the line memory. When an image requires reduction, it is sent to the line memory for buffering prior to being sent to main memory. Gate array 1 also provides these

additional functions:

- Address generation
- Memory control
- Bus interface
- Grayscale horizontal-resolution conversion
- CCD control

The PEL correction memory and line memory (2-Kbytes RAM) are used to buffer data from the DIPP before transfer to main memory.

Gate array 2 is used to support these functions of the DIPP:

- DMAC (two channel)
- Bus arbitration
- interrupt control
- Carrier arm-motor control
- Address latch
- Chip-select control

The microprocessor logic controls the functions of the gate arrays, DMAC, and carrier arm-motor control. The scanner uses an 8-bit NEC (7809) microprocessor. This processor runs at a 12-MHz clock rate and is supported by 256 bytes of RAM, an input/output port, a timer, and interrupt circuitry.

The clock-generation circuitry provides all the necessary timing pulses for the circuits in the scanner. The scanner has 2 separate clocks, a 12-MHz which is used by the microprocessor, and an 8-MHz clock used by gate array 2. Also, the 8-MHz clock is divided by 2 to provide a 4-MHz clocking for the DIPP, gate array 1, and the DMAC.

Main memory of the scanner contains two 16-Kbyte banks of RAM and 32-Kbytes of ROM. The ROM firmware is used to control the scanner, while the two banks of RAM are used to buffer the image data and provide the microprocessor with working space for parameter information.

The DMAC IC is used to improve the scanners performance by off-loading the burden of data transfer from the microprocessor. This process results in faster data transfer between the scanner and the host system.

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