68040 CPU Architecture: NuBus Transfer Modes and Performance

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TOPIC -----

Can you give information about the architecture of the 68040 CPU? It isn't clear which master/slave transfer modes are supported in the 68040 computer between the host and the NuBus. What would the NuBus Block Transfer Modes Resource Entries look like for the 68040 computer per the DTS Technical Note #288? What performance can we expect?

DISCUSSION -----

The Macintosh Quadra computers support all sizes of block transfers when the main logic board is accessed as a slave device. (The NuBus specification states that if a slave accepts any block transfer, it must accept all block transfers.) As a NuBus master, the Quadra doesn't initiate block transfers. NuBus masters don't have to support all sizes of block transfers.

The data rate a NuBus master will see when doing block transfers to the main logic board is 8 to 10 MB/sec, depending on main memory refresh cycles and synchronization delays. This is a maximum rate that can be achieved only if the NuBus master does nothing but block transfers (that is, it moves data continuously without doing any other operations). A more realistic maximum rate is 4 to 5 MB/sec.

When the main logic board is the bus master, the transfer rate depends greatly on the speed of the NuBus slave device. A zero wait state NuBus slave (none of which exist as far as we know) could give peak transfer rates approaching 20 MB/sec. Real NuBus slave devices will probably have transfer rates under 10 MB/sec (more like 2 to 4 MB/sec). The only way to really determine how fast a Quadra can transfer data to a NuBus slave is to run real code and time the bus transfers.

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