Macintosh Quadra 950: Integrated Circuits (6/94)

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TOPIC ----------

The circuitry of the Macintosh Quadra 950 computer has many new features along with older features it shares with the Macintosh IIci and IIfx computers. Certain components appeared for the first time in the Macintosh Quadra 900, and are therefore present in the Quadra 950 as well:

- The MC68040 microprocessor
- Several new custom ICs
- The built-in video hardware
- The 68040 PDS slot.

This section describes the circuit design of the Macintosh Quadra 950.

DISCUSSION ----------

There are three buses in the Quadra 950 computer:

- System bus
- I/O bus
- NuBus

The system bus connects directly to the pins of the MC68040 microprocessor and runs at the processor's clock rate of 33 MHz. The system bus is a high performance bus, with the capability to read burst-read and burst-write. Five controller ICs are connected to the system bus:

- Orwell, the custom memory controller
- YANCC, the NuBus controller
- DAFB, the frame-buffer controller
- The two 53C94 SCSI controllers

The I/O bus in the Quadra 950 computer is similar to the I/O bus in the Macintosh IIfx computer. The I/O bus in the Quadra 950 computer runs at a clock rate of 25 MHz. The controller ICs that are connected to the I/O bus include new custom ICs along with ICs originally designed for the Macintosh IIfx, such as the IOPs.

The NuBus runs at a clock rate of 10 MHz and includes several features of NuBus '90, including a clock signal at 20 MHz between cards, which is twice the normal rate. This clock rate doesn't apply from card to CPU.

Integrated Circuits (ICs)

The Quadra 950 incorporates all of the same ICs that the Quadra 900 did, many Apple custom ICs, and some new ASICs.

The Apple custom ICs that the Quadra 950 computer shares with earlier Macintosh models include:

- AC/DC: a custom Color Look-Up Table and Digital-to-Analog Converter (CLUT/DAC) IC developed by Apple and used in the Macintosh Display Cards 4•8, 8•24, and 8•24 GC, but improved in the Quadra 950.
- DFAC (Digitally Filtered Audio Chip): the sound input and filter IC first used in the Macintosh LC
- IOP: the I/O processors first used in the Macintosh IIfx
- SWIM: the IC that supports the SuperDrive disk drive

The Apple custom ICs that are newly designed for the Quadra 950 computer are:

- BATMAN: a custom IC (replaces the Apple Sound Chip) that acts as a sound amplifier
- SPORTY: a custom IC that provides sound output functions
- CABOOSE: a custom processor that manages system power, the real-time clock, and parameter RAM
- DAFB (Direct Attach Frame Buffer): an IC that connects directly to the system bus and controls the video RAM or frame buffer
- ORWELL: a custom IC that connects to the system bus and controls burst-mode data transfers to the main RAM
- JDB (Junction Data Bus): one of two ICs making up the I/O Adapter, connecting the data signals from the system bus and the I/O bus
- RELAYER: one of two ICs making up the I/O Adapter, controlling the bus buffers and proving bus arbitration logic
- YANCC (Yet Another NuBus Controller Chip): a custom IC that controls the NuBus interface

Third-party ICs include:

- SCSI interface ICs: two NCR 53C96
- Sonic: the DP83932 Ethernet controller IC made by National Semiconductor
- Two VIAs similar to those in earlier members of the Macintosh II family

I/O bus adapter ICs: JDB and Relayer

The I/O bus attaches local I/O devices to the system bus in a way that is flexible and highly compatible with previous Macintosh systems, and is fully buffered from the system bus to reduce capacitive loading. By putting Relayer and JDB between the system bus and I/O bus, none of the 040 signals go directly to the I/O chips, thus reducing the loading on the 040 bus signals, and increasing speed and reliability. The I/O bus hardware

protocols are a subset of the 68030 bus protocols.

The two-chip set consisting of the Relayer and JDB provide a transparent connection between the system bus and the I/O bus. The I/O bus enables the Quadra 950 computer to use the same I/O device controllers used in the Macintosh IIfx. The I/O bus clock runs at 24.28 MHz and is completely asynchronous to the system bus clock.

This two-chip setup allows any system bus master such as the 040, a NuBus master card, or a master device on the PDS to request bus access and transfer data to slaves located on the I/O bus. It also allows I/O bus masters like SONIC to access main memory which is located on the system bus. This improves the overall speed of the system by isolating the faster bus (system bus) from the slower bus (I/O bus).

The I/O bus adapter is made up of two ICs: JDB and Relayer. Two ICs are used because of the high pin count required.

The functions of the Relayer IC include:

- Generating chip select and DSACK signals for devices on the I/O bus
- Converting timing signals between the system bus and the I/O bus
- Arbitrating between the system bus and the I/O bus
- Acting as watchdog for bus activity and time out
- Controlling the address-bus transceiver ICs
- Generating the clock signal for the VIA ICs

The functions of the JDB IC include:

- Controlling the data path (dynamic bus sizing and data byte lane routing)
- Synchronizing and distributing the reset signals

The ICs making up the I/O bus adapter contain no programmable registers and don't require support from the system software.

Memory Controller IC: Orwell

The Orwell IC connects to the system bus and provides control and timing signals for RAM and ROM. The Orwell IC supports all types of MC68040 memory access, including burst modes. Orwell allows all memory to be marked cache-able, which means cache-inhibit isn't asserted.

When the computer is reset, the Orwell IC maps ROM addresses into memory beginning at address $0000 0000 and disables the system RAM. As soon as the ROM code addresses the normal ROM space ($4000 0000), the Orwell IC automatically remaps the ROM to its normal addresses and restores RAM addressing starting at $0000 0000. The microprocessor always starts upon reset at address 0. At that time there is nothing in RAM (which resides at address 0 after reset). Therefore, ROM code needs to be accessed, and since its normal addressing starts at $4000 0000, it's remapped down so the processor has some code to fetch upon reset. This is the same process in every Macintosh II.

RAM Control

The Orwell IC controls four banks of dynamic RAM. Each bank accepts standard 80ns SIMMs containing 1MB, 4MB, and perhaps 16MB (256K and 2MB aren't supported), giving total memory sizes from 8MB to 16MB for each bank (256MB if 16MB SIMMs work). Therefore, the Quadra 950 could have a total of 64MB when using the SIMMs currently available. 16MB SIMMs haven't been thoroughly tested on the Quadra 950, and therefore can't be listed as a possible configuration. The Quadra 950 can also use 60ns SIMMs, but Orwell is programmed for 80ns DRAM, so a 60ns SIMM wouldn't improve the speed. If one slot in a given bank is filled, then all slots in the bank must be populated.

Note: When large amounts of DRAM are installed, the memory check upon startup is lengthy and can cause users to think that the computer isn't functioning. There is no software indication that the computer is running memory checks.

The Orwell IC contains registers that the system software uses to set the starting address of each bank of memory. At startup, the system software determines the sizes of the banks and assigns the bank starting addresses so that the banks occupy contiguous memory spaces, unlike that of the Macintosh IIci and IIsi, which have split memory maps.

ROM

The ROM in the Quadra 950 is soldered directly to the main logic board, and consists of two 4MBit ROMs at 150ns (each ROM is a 256K x 16 device)=1MB ROM. As with all instructions, ROM can be cached in the 040. The memory controller, Orwell, supports burst access to the ROM via the 68040 fake burst mechanism. This means that Orwell asserts Transfer Burst Inhibit (TBI) with TA for accesses to ROM, which can't be "bursted." This allows the 040 to try a burst, and then notice that it must do the accesses in four individual long words.

SCSI Controller ICs

In the Quadra 950, the SCSI bus is divided into internal and external buses, each controlled by its own NCR 53C96 device. The internal and external SCSI buses are logically connected, but electrically separate. The external bus is electrically isolated from the internal bus so that changes in external cabling and termination have no effect on the performance of the internal SCSI devices.

The cabling and termination of the internal SCSI bus are optimized so that the 53C96 that controls the internal bus can support data transfers at a faster rate -- up to 5MB/s (the maximum the chip can transfer is 6MB/sec). Earlier Macintosh computers were capable of a 3MB/s transfer rate.

NuBus Controller IC: YANCC

In the Quadra 950 computer, the interface between the system bus and the NuBus comprises three chips: the YANCC IC and two 16-bit transceiver ICs

that are the same as the ones in the Macintosh IIci.

The YANCC IC maps certain system bus cycles to NuBus cycles and certain NuBus cycles to system bus cycles. The features of the YANCC IC include:

- Support for all types of single data transfers in either direction
- A buffer, one long word deep, for appended writes from the MC68040 to the NuBus
- Support for block move transfers between NuBus masters and main memory
- Support for pseudo-block transfers between the MC68040 and NuBus slaves
- Support for some new functions defined in the NuBus '90 specification

Unlike the NuBus controllers in previous Macintosh computers, the YANCC IC generates an interrupt when there is an error involving the write buffer. Software controls this interrupt by means of a control and status register in the YANCC.

Video Frame-Buffer Controller IC: DAFB

The built-in video hardware in the Quadra 950 computer provides high-performance graphics on all current Macintosh monitors. The video hardware is built around a video frame buffer controlled by the DAFB IC.

The video frame buffer comprises four banks of video RAM (VRAM); two of which are soldered onto the logic board. This minimum configuration (1MB soldered on) supports 16 bits per pixel on all Apple monitors up to 16 inch, and 8 bits per pixel on all Apple monitors. The basic VRAM configuration supports 24 bits per pixel on the 12-inch RGB monitor. The standard 1MB VRAM also supports NTSC and PAL monitors, using Apple convolution as well as VGA monitors. By installing VRAM SIMMs into the other two banks (four 256K VRAM SIMMs), the user can expand the frame buffer to support 24 bits per pixel for the 13-inch and 16-inch monitors.

Because the frame buffer in the Quadra 950 computer is connected directly to the system bus, which is now even faster than the Quadra 900, it speeds up all applications, even those that don't use QuickDraw. Given the faster clock speed, and the removal of wait states in the VRAM timing, the Quadra 950 frame buffer can perform graphic operations, such as scrolling, up to 50% faster than the Quadra 900 frame buffer.

The control registers in the DAFB IC and the frame-buffer VRAM are mapped into the memory locations that were assigned to NuBus slot $9 in earlier models.

Sound ICs: DFAC, Batman, and Sporty

The Quadra 950 computer uses a new sound system. Its features are similar to the features of the sound interface in the Macintosh LC and the IIsi. The features of the Quadra 950 sound interface include:

- ASC compatibility
- Ability to play 8-bit sound files
- 8-bit sound input

- Lower noise and distortion analog circuitry

Four Apple custom ICs provide the sound interface:

- DFAC: provides sound input and an anti-aliasing filter
- Batman: an updated version of the Apple Sound Chip
- Sporty: a custom IC that replaces the two Sony sound ICs
- External digital-to-analog converter (DAC)

The Digitally Filtered Audio Chip (DFAC) is an Apple custom IC that is also used in the Macintosh LC. The DFAC IC includes the anti-aliasing filter and analog-to-digital converter (ADC) for sound input. It also contains a digital filter for conditioning output data before it is sent to the DAC. The DFAC serializes the sound input information and sends it to Batman, where it is put into a FIFO, which software can read.

The Batman sound chip provides ASC compatibility and includes several important new features such as support for sound input, support for an external D/A converter, and large FIFOs which buffer playback and sound input samples. Batman doesn't support the wave table function which was available in the original ASC (this feature was not widely used and should only cause very limited compatibility problems). The Batman transfer acknowledge is generated by Relayer.

For sound output, an external DAC provides higher-quality sound than that generated by the PWM system used in earlier Macintosh models. The Sporty custom IC replaces the two Sony ICs used in earlier models and provides better sound quality (that is, less noise and distortion). Like the Sony ICs it replaces, the Sporty IC also contains digital attenuators. A separate amplifier with power output of 2 watts drives the larger speaker used in the Quadra 950 computer.

Article Change History
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30 Jun 1994 - Revised formatting.
09 Dec 1992 - Corrected to remove statement saying you cannot mix RAM speeds in different banks.

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