Centris 610 & 650, Quadra 800: Custom ICs (7/94)

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TOPIC ---

There are three new custom ICs introduced with the Centris 610, Centris 650, and Quadra 800:

- DJMEMC: Dale & Jay's Most Excellent Memory Controller
- IOSB: Input/Output Subsystem Buffer
- KIWI: NuBus Controller

These three ICs integrate functions provided by the ten custom ICs found on the Quadra 700 logic board. This article describes each of these ICs in detail.

The information in this article relative to the Centris 610 and Centris 650 is also relevant to the Quadra 610 and Quadra 650.

DISCUSSION ---

Note: The Centris 610, Centris 650, and Quadra 800 also include a number of ICs developed for previous Macintosh models. Although not described in this article, they are:

- DFAC: Sound - Input and File
- MC68040: Microprocessor
- AC843: CLUT/DAC
- Antelope: Low cost CLUT/DAC
- MCCS142235: Active SCSI Terminator
- DP8534: Video timing generator
- SONIC: Ethernet controller
- 53C96: SCSI controller

DJMEMC (Dale and Jay's Most Excellent Memory Controller)

DJMEMC is a very large-scale IC that combines functions performed by multiple devices in previous Macintosh designs. DJMEMC attaches to the system bus and provides the control and timing signals for the RAM, ROM, and VRAM. It also controls the logic that controls the system bus arbitrations that provide the video timing and control signals. In summary, key functions provided by the DJMEMC are:

• Address decode
• Bus arbitrator
• Configuration register
• DRAM/ROM controller
• System bus interface
• Video timing
• VRAM controller

DJMEMC also includes a complete video frame buffer controller for a VRAM-based frame buffer which supports high performance graphics. Essentially, all of the DAFB frame buffer controller used in the Quadra 700, 900, and 950 have been incorporated into DJMEMC. Therefore DJMEMC is capable of supporting all of the display options and configurations supported by the Quadra 700, 900, and 950. This frame buffer also makes use of two new devices: the National DP8534 clock generator, and the Antelope CLUT/DAC. The 8534 (not compatible with the DP8531 used by the earlier Quadra computers) generates all video clock frequencies needed, up to and including 100 MHz. Antelope is a significantly cost-reduced version of the AAC, and does not include support for 24 bpp or Apple convolution. Antelope is pin- and software-compatible with the AAC used by the Quadra 950.

IOSB (I/O Subsystem Buffer)

IOSB performs some of the functionality found in the JDB/Relayer two-chip set used in the Quadra 700, 900, and 950 -- and also integrates a number of the discreet components which were located on the Quadra 700, 900, and 950 I/O bus.

The key functions of the IOSB ASIC are:
• Byte steering
• Bus sizing
• Alternate I/O bus masters
• Device decode logic
• CPU ID register
• Sound
• VIAs
• SWIM2
• Power on circuit
• System watchdog timeout
• Interrupts

Byte Steering: The 68040 does not support data steering. However, the 68030 allows 8-bit and 16-bit slaves to attach to a given byte lane and indicate their port size during cycle acknowledge. Hardware in the 68030 bus interface did the appropriate byte steering. This allows S/W to do byte accesses to consecutive bytes in 8-bit devices like the SCC without any external logic. In order to maintain compatibility with existing software, the IOSB ASIC does byte steering for 68040 accesses to I/O bus peripherals.

Bus Sizing: The 68040 does not support dynamic bus sizing; it expects accesses to 8-bit and 16-bit ports to be of the appropriate size, that is access.B for 8-bit ports and access.W for 16-bit ports. However, the 68030 allows 8-bit and 16-bit slaves to attach to a given byte lane and indicate their port size during

cycle acknowledge. The hardware inside the 68030 does the appropriate number and type of bus cycles to fulfill the request. This allows long word accesses to 8-bit devices, like the SCC. To maintain compatibility with existing software, IOSB does dynamic bus sizing for 68040 accesses to I/O bus peripherals.

Alternate I/O Bus Masters: IOSB allows the SONIC Ethernet controller to be a bus master on the System bus. SONIC drives the System bus snoop control bits (SC1 and SC0) directly, while IOSB drives the TT control lines. The status of these bits is determined by a register within SONIC, and should be initially configured not to snoop.

IOSB does not support true burst transfers to the I/O bus. If a System bus master attempts to burst data to or from an I/O bus slave, IOSB will invoke a 68040 fake burst. This allows use of the MOVE16 instruction for I/O bus data. IOSB itself does not initiate burst cycles on the System bus.

Device Decode Logic: IOSB provides device selects according to the memory maps shown earlier. It provides chip select for all I/O bus devices (that is, Ethernet PROM, patch ROM, SCC, SCSI, and SONIC) and internal IOSB cells (that is, VIAs, SWIM2, sound, and ADB). Note that DJMEMC and KIWI provide their own chip selects.

Sound: IOSB provides a variation of the sound controller used in the Sonora ASIC (used on the Macintosh LC III). However, instead of using DRAM or VRAM for sound I/O buffers, IOSB will internally provide 3K of internal static RAM.

Separate 1-Kbyte buffers are provided for left sound output, right sound output, and mono sound input. Since a sound output buffer is not reused for sound input, IOSB will be capable of providing simultaneous stereo sound output while recording from the sound input port. Sound buffers internal to IOSB are required for maximum software compatibility with Apple and third-party sound drivers.

VIAS:IOSB includes two VIAs, similar to the original Macintosh II. The VIA clock is generated within IOSB. VIA1 is the same VIA cell used in VISA, V8, Sonora, and PSC. It has full Macintosh VIA capabilities. VIA2 is a variation of the cell used in VISA, V8, etc.... This is not a complete VIA, but performs all the functions required from VIA2 (mostly interrupt support and some read/write port bits).

SWIM2:IOSB contains the SWIM2 floppy disk controller. It has full Macintosh SWIM2 capabilities, and is capable of supporting a 2.88MB floppy format.

Power-On Circuit: The Centris 610, Centris 650, and Quadra 800 use the same power-on logic as the Macintosh IIci. However, the portions of the power-on circuitry that do not run off the +5V trickle supply have been moved into the IOSB ASIC to reduce component count on the motherboard.

System Watchdog Timeout: IOSB includes timeout logic that monitors system bus activity and terminates faulty cycles with a bus error indication. This timer does not run when an access is made to a NuBus device; it assumes that the NuBus controller will include a timer which handles the (longer) NuBus timeout period

(25.6 µsec).

IOSB also maintains a watchdog timer for the entire system, including NuBus. This timeout has a longer period than previous timers, and prevents "hanging" while waiting for a response from a damaged or non-existent device. For instance, this timer would catch PDS cards that do not respond to all accesses to NuBus slot E space (see YANCC description for more information on PDS decoding).

Interrupts: IOSB will terminate all 68040 interrupt acknowledge cycles with autovector indication. Like the Quadra 700, 900, and 950, the Centris 610, Centris 650, and Quadra 800 allow separate mappings for different operating systems.

IOSB also provides for multiple modes of operation to support the use of IOSB in future CPUs, and to provide a failsafe mechanism in case of problems during development. These options include:

- Internal/external sound (allows use of the EADSC for higher quality sound output)
- Internal/external SWIM

KIWI

The KIWI ASIC provides the interface between the System bus and NuBus. It combines the functions that were provided by the YANCC ASIC, two bus transceivers, and several discrete driver chips. KIWI provides a complete 68040 bus interface on one side and a complete NuBus interface on the other.

Key functions provided by the KIWI ASIC are:
- Support for all types of single transfers
- One longword deep buffer
- Support for block move transfers for NuBus masters accessing memory on the motherboard
- Pseudo-block transfers from the 68040 to NuBus slaves
- Several of the new functions being defined by NuBus 90 spec

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28 Jul 1994 - Added reference to Quadra 610 and 650 to aid in searching.

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