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Centris 610 & 650, Quadra 800: NuBus Information (7/94)

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TOPIC -----

What are the changes in the NuBus implementation in the Macintosh Centris 610, Centris 650, and Quadra 800? How does each system support it?

The information in this article relative to the Centris 610 and Centris 650 is also relevant to the Quadra 610 and Quadra 650.

DISCUSSION -----

NuBus Implementation

The NuBus implementation in the Centris 610, Centris 650, and Quadra 800 utilizes the same signals used in previous Quadra computers. These NuBus slots utilize many of the features specified in the NuBus90 standard.

NuBus '90 is the 1990 proposal for revision of the IEEE standard for the NuBus (IEEE STD R1196-R-1990). Apple has a representative on the panel designing the new standards, and has had since its inception. The specifications for NuBus '90 are incomplete and still under development, but Apple has implemented the portion of the specifications that are completed, and will be updating the implementation as the specs expand and stabilize. The NuBus slots in the Centris 610, Centris 650, and Quadra 800 provide the following new features described in that proposal:

- Low current at +5 V is available on the new STDBYPWR pin when main power is off and the AC cord is plugged in.
- New signals /TM2, /CLK2X, and /CLK2XEN support block transfers at double the standard rate (20 MHz). Double-rate block transfers are supported between NuBus cards, but does not transfer to or from the main memory (this remains at 10 MHz).
- NuBus '90 defines new signals SB0 and SB1 for a serial bus on the formerly reserved pins A2 and C2. The serial bus signals are bused and terminated, but the main circuit board does not drive them.
- NuBus '90 defines new signals /CM0, /CM1, /CM2, and /CBUSY to support a cache coherency protocol. Pins on the NuBus connector are assigned to

those signals, but the current systems do not support them.

The following table lists the new signals described in the proposal for NuBus 90.

NuBus '90 signals on the NuBus connector

Pin #	Signal name	Function
A2	SB0 !	High-speed serial bus, defined in P1394 proposal.
C2	SB1 !	High-speed serial bus, defined in P1394 proposal.
B8	/TM2	New transfer mode: requests double-speed transfer.
B9	/CM0 !	For cache-coherency operations.
B10	/CM1 !	For cache-coherency operations.
B11	/CM2 !	For cache-coherency operations.
B24	/CLK2X	Synchronizes double-speed block transfers.
B25	STDBYPWR	Small current at +5 V when main power is off; enables the card to turn main power on by asserting /PFW signal.
B26	/CLK2XEN	If not connected to other NuBus '90 signals, this line enables /CLK2X driver.
B27	/CBUSY	Used with cache-coherency operations.

! - These signals are not driven or monitored.

CPU NuBus Support

The Centris 610 has one expansion slot, which can be used by a PDS adapter or by a NuBus adapter similar to the one used in the Macintosh IIsi. This expansion slot is a 140-pin dual position edge connector. The NuBus adapter contains the NuBus interface circuitry and has a single NuBus connector.

NuBus cards must follow the small-size NuBus standard: a maximum of seven inches long and use a maximum 10W of power. NuBus cards that follow the seven-inch standard can be used in any NuBus-equipped Macintosh.

The Centris 650 and Quadra 800 each support three NuBus slots, one more than the Quadra 700, that may draw up to 15W each. These NuBus slots are addressed as \$C, \$D, and \$E. The PDS slot lines up with slot \$E, either the PDS slot or slot \$E may be used -- but not both.

A single chip, the KIWI ASIC, provides the interface between the system bus and NuBus.

For Further Information

For further details on the KIWI ASIC, see the related Tech Info Library article "Macintosh Centris 610, Centris 650, Quadra 800: Custom ICs".

For complete specifications and a discussion of NuBus, refer to Developing Cards and Drivers for the Macintosh Family, third edition.

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