Macintosh IIci: Calculating RAM Speed

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TOPIC ---

Why is the RAM on the Macintosh IIci 80ns? My own mathematical calculations suggest a required speed of 40ns for a 25MHz chip and no wait states.

DISCUSSION ----------------------------------

Your math is correct: the 25MHz 68030 CPU clock has a period of 40ns per clock.

However, the minimum memory access cycle for Macintosh IIci is two clocks, which means that there is at least 80ns between memory accesses (one wait state). The maximum number of cycles between memory accesses is five clocks (three wait states).

For example, the Macintosh IIci performs a random read from DRAM in five clocks and a four long word burst read in 11 clocks -- five clocks for the first long word and two clocks each for the remaining three long words.

   1st Long Word - 5 clocks or 3 wait states
   2nd Long Word - 2 clocks or 1 wait state
   3rd Long Word - 2 clocks or 1 wait state
   4th Long Word - 2 clocks or 1 wait state

Keywords: <None>

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