Macintosh IIci: RAM Requirements

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Article Change History

09/30/92 - UPDATED

- To include additional information on the use of burst mode with Fast Page Mode RAM.

TOPIC ----------

This article explains the RAM requirements of the Macintosh IIci. Part numbers for Apple labeled SIMM upgrades and service parts that meet these requirements are also included.

DISCUSSION ----------

The increased speed of the Macintosh IIci is primarily due to two factors. The first factor is the increased speed of the 68030 CPU and 68882 FPU. Those chips are clocked at 25 MHz in the IIci.

The second is that the Macintosh IIci support 68030 burst reads to the on-chip data and instruction caches.

The 256 byte 68030 data and instruction caches are each organized in sixteen lines of four long word entries. The 68030 can save cacheable instructions or data into these long word entries. When burst mode is disabled, it takes five processor cycles to fetch each long word entry into the cache. Each entry is read into the cache, one at a time, as needed. To fill an entire cache line would take twenty cycles (5 + 5 + 5 + 5 = 20 cycles).

When burst mode is enabled, the on-chip cache entries are filled one line at a time. It takes five cycles to fetch the first entry, but it takes only two cycles to fetch each of the remaining three entries, resulting in a total of eleven cycles to fill the entire cache line (5 + 2 + 2 + 2 = 11 cycles). This mode is sometimes referred to as the "5 2 2 2" burst mode.

To satisfy the timing requirements of the 25 MHz 68030, the IIci requires a RAM speed of 80 ns or faster. To satisfy the requirements for burst

reads, the IIci requires RAM that has a Fast Page Mode access type. Fast Page Mode (FPM) is a RAM access type that is necessary to support the "2 2 2" portion of the "5 2 2 2" burst mode access.

The use of burst mode with Fast Page Mode RAM gives the processor a maximum RAM access rate of 36.36 MB/sec. That access rate is always true for bank B. For bank A, it is achieved only when not using the built-in video circuits on the logic board; using a NuBus video card.

The built-in video circuits use a video buffer in RAM bank A. The effect of the video RAM cycles can decrease the processor's access to bank A by as little as 6% or as much as 65%, depending on the type of video display in use. Larger displays and display modes with more bits per pixel have a greater effect.

You will obtain better performance when using the built-in video circuitry by installing the larger SIMMS in bank B. For example, in a 5 MB configuration, put the 256KB SIMMS in bank A and the 1 MB SIMMS in bank B.

Ultimately, maximum performance can be achieved by adding a NuBus video card (high end / co-processor type).

If RAM is used in the IIci that is slower than 80ns, or does not support fast page mode, the system will eventually crash. Most of the RAM SIMM modules that are 80 ns have a Fast Page Mode access type. As a result, it should be uncommon for users to unknowingly install RAM in the IIci that do not have this access type. However, it is likely that unknowing or curious users will install RAM SIMMs that are rated slower than 80 ns. In most cases, those users will find that the slower RAM may work for a short time, but the IIci unit WILL eventually crash with a serious system error.

There are several reasons why a Macitosh IIci will not always crash immediately on power up when slower RAM is installed. They include:

- Frequently, RAM speed is rated conservatively. As a result, a chip may actually be faster than it is rated under certain circumstances.

- Many of the RAM SIMMs that are available on the market for use in the Macintosh SE/30, II, IIcx and IIx, including some sold by Apple, are rated for 100 ns, which puts them close to the 80 ns requirements.

- RAM speed is higher in a cooler chip than in a warmer chip with the same rating. When the Macintosh is first turned on, the chips are cool. After the unit is turned on, the chips will heat up, which causes them to slow down.

The part numbers for Apple labeled SIMM upgrades and service parts that meet these requirements are listed below.

Finished Goods RAM Upgrade Packages:

Finished Goods Upgrade Size	Part Number

1MB, 80 ns FPM	M0291LL/A
4MB, 80 ns FPM	M5952LL/A
4MB (Parity), 80 ns FPM	M0294LL/A

Service Goods RAM SIMM Parts:

Service RAM Density	Part Number
256KB, 80 ns FPM	661-0519
1MB, 80 ns FPM	661-0520
1MB (Parity), 80 ns FPM	661-0546

To identify 80 ns chips, some RAM manufacturers indicate RAM speed on the chip with a number that is usually expressed in tens. For example, 80 ns chips are marked with an 8, 100 ns with a 10, 120 ns with a 12 and 150 ns with a 15. When the speed is marked on the chip, it is usually set apart from the chip part number with a dash or is positioned in a separate location on the surface of the chip. Also, some SIMM manufacturers indicate the RAM speed on the back of the SIMM board.

For most of the SIMM modules that Apple sells, RAM speed can be identified with one of the above methods. However, RAM speed of some third-party SIMM modules are not so explicitly marked on the chips or the SIMM board.

Identifying RAM that supports fast page mode is more difficult, because this characteristic is usually not explicitly printed on the chip or the SIMM board. In most cases this will not be a problem, because the vast majority of the 80 ns DRAM SIMM can be installed into a IIci support Fast Page Mode.

Although both of these pieces of information can be confirmed in the chip manufacturers' data book, most people will prefer to contact the SIMM vendor to verify that the modules are compatible with the IIci. Customers should avoid purchasing SIMMs that cannot be confirmed to be IIci-compatible.

Many of the 256KB SIMM modules for the IIci will look different from the SIMM modules that we are accustomed to. Until now, Apple labeled RAM SIMM modules have contained eight RAM chips (8 chips x 256K x 1-bit each). Most of the Apple labeled 256KB, 80 ns, fast page mode RAM SIMMs will have only two RAM chips (2 chips x 256K x 4-bits each). Each SIMM module contains 256KB, but each chip contains four bits of each byte, instead of just one bit.

The 256K x 4-bit chips were chosen because 256K x 1-bit, 80 ns, fast page mode chips are not readily available.

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