Macintosh IIfx: Input/Output Processors (IOP) Chips

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TOPIC ---

This article describes the Macintosh IIfx's Input/Output Processors (IOP) Chips.

DISCUSSION --

The I/O Processor (IOP) is an Apple custom IC designed to provide intelligent support for I/O controllers. There are two of these IOP chips in the Macintosh IIfx computer: one for the SWIM and ADB and one for the SCC. The IOP sits between the main processor and the I/O controllers. The features of the IOP include:

- A built-in microprocessor (6502 running at 2 MHz)

- A 17-bit timer

- Two DMA controllers: one for each serial I/O channel (only used in the Serial IOP)

- Address and data busses for RAM used by the IOP and host processor

- Two digital I/O ports for controlling the ADB (on the SWIM-ADB IOP)

- 32K of external memory of IOP code and data storage

The 68030 communicates with the IOP through a set of control registers in the IOP that are mapped into the main processors' I/O space. The main processor can interrupt the IOP using a bit in one of the control registers, whereas the IOP can interrupt the 68030 by using an interrupt line.

Each IOP has 32K of external RAM that holds the driver and acts as a buffer for the data processed by the processor. The IOP contains a 16-bit auto-incrementing address register and an 8-bit data port that the host processor uses for access to the shared RAM.

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