Apple IIc: Description of Video Expansion Port

The back panel of the Apple IIc has a DB-15 connector for sophisticated video interfaces external to the computer. See the table below for a description of signals.

In the table, the column labled Deriv indicates from which clock signals the video signals are derived. LDPS, CREF and PRAS have a maximum delay of 30ns from the appropriate 14MHz rising edge. SEROUT is clocked out of a 74LS166 by the rising edge of 14M and has a maximum delay of 35ns. VIDD7 is driven from a 74LS374 and has a maximum delay of 28ns from the rising and (if 80 column) falling edges of phase1.

To align CREF so it is in the same phase at the beginning of every line, certain clock signals must be stretched. This stretch is for one 7M cycle (140ns), and occurs at the end of each video line. All timing signals except 14M, 7M and CREF are stretched.

WARNING!!! The signals at the DB-15 on the Apple IIc are not the same as those on the Apple III. Do not attempt to plug a cable intended for one into the other.

WARNING!!! Several of these signals, such as 14MHz, must be buffered within about four inches (10 cm) of the back panel connector - preferably inside a container directly connected to the back panel.

The Video Expansion Connector Pinouts

Pin	Deriv	Name	Description
1	phase1	TEXT	Video text signal from TMG; set to inverse of GR, except in double high-resolution mode
2		14M	14M master timing signal from the system oscillator
3	Q3	SYNC*	Display horizontal and vertical synchronization signal from IOU pin 39
4	PRAS	SEGB	Display vertical counter bit from IOU pin 4; in text mode indicates second low-order vertical counter; in graphics mode indicates low-resolution

5		1VSOUND	One-volt sound signal from pin 5 the audio hybrid circuit (AUD)
6	14M	LDPS*	Video shift-register load enable from pin 12 of TMG
7	PRAS	WNDW*	Active display area blanking; includes both horizontal and vertical blanking
8		+12 V	Regulated +12 volts DC.; can drive 350mA
9	14M	PRAS*	RAM row-address strobe from TMG pin 19
10	PRAS	GR	Graphics mode enable from IOU pin 2
11	14M	SEROUT*	Serialized character-generator output from pin 1 of the 74LS166 shift register
12		NTSC	Composit NTSC video signal from VID hybrid chip
13		GND	Ground reference and supply
14	phase0	VIDD7	From 74LS374 video latch; causes half-dot shift if high
15	14M	CREF	Color reference signal from TMG pin 3; 3.58MHz

WARNING!!! Use caution. The maximum allowable current drain of +12V regulated power at the video expansion connector is 300 milliamps. If the external device draws more than this it can damage the computer or cause the power supply to shut down.
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