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Communications Interface: Directly controlling the 6850 ACIA

This applies to the Apple II, II+, and IIe.

The Communications Interface Card uses an ACIA (Asynchronous Communications Interface Adapter) to automatically perform the serial transfers with an external device. The ACIA contains 4 registers that control data flow between the Apple and the external device. There are two pairs of registers and each pair has a single address in the Apple. In the following discussion, all addresses will be calculated for slot 2. The addresses can be converted to another slot with the following formula.

$$\text{New Address} = \text{Old Address} + (\text{New Slot} - 2) * 16$$

So, \$C0AE in slot 2 becomes \$C09E for slot 1.

The status/control register is at \$C0AE. Reading from \$C0AE yields the status of the ACIA, and writing to \$C0AE modifies the Operation of the ACIA (baud rate, data bits, stop bits, parity). The tables below are a summary of what the registers control. Refer to the Motorola Semiconductors Data Sheet for the MC6850 for complete details.

READ FROM STATUS REGISTER (\$C0AE)

- 0 Receive Data Register Full
- 1 Transmit Data Register Empty
- 2 -Data Carrier Detect
- 3 -Clear to Send
- 4 Framing Error
- 5 Receiver Overrun
- 6 Parity Error
- 7 Interrupt Request

WRITE TO CONTROL REGISTER (\$C0AE)

- 0-1 Baud Rate
 - 0 - Unstable at about 1200 baud
 - 1 - 300 baud
 - 2 - 110 baud
 - 3 - Reset the ACIA
- 2-4 Word Control Bits
 - 0 - 7 bits + Even Parity + 2 Stop Bits

- 1 - 7 bits + Odd Parity + 2 Stop Bits
- 2 - 7 bits + Even Parity + 1 Stop Bit
- 3 - 7 bits + Odd Parity + 1 Stop Bit
- 4 - 8 bits + 2 Stop Bits
- 5 - 8 bits + 1 Stop Bit
- 6 - 8 bits + Even Parity + 1 Stop Bits
- 7 - 8 bits + Odd Parity + 1 Stop Bits

5-6 Transmitter Control Bits

- 0 - -RTS = low, Transmitting Interrupt Disabled
- 1 - -RTS = low, Transmitting Interrupt Enabled
- 2 - -RTS = high, Transmitting Interrupt Disabled
- 3 - -RTS = low, Transmits a Break level on the Transmit Data Output.
Transmitting Interrupt Disabled

7 Receive Interrupt Enable Bit

- 0 - No interrupts from receiver section of ACIA
- 1 - Interrupt on:
Receive Data Register Full,
Overrun, or
A low to high transition on Data Carrier Detect

The data register is located at \$C0AF. A read from \$C0AF yields the data that has been received from the external device. A write to \$C0AF buffers the data and initiates its transmission. Writing or reading to the data register automatically resets the ACIA status.

An Apple II will lose data whenever it is forced to ignore the Communications Interface to either process the incoming data or write it to an I/O device like a disk drive or printer.

This problem is solved by buffering the incoming data. You can do this by:

- 1) Requesting fixed size blocks of data from the remote machine - Reading in all of one block and processing it before requesting the next one.
- 2) Writing a program to control the data flow from the remote device with XON (control S) and XOFF (control Q). The strategy is to receive data until the program's memory buffer is almost full and transmit an XOFF to halt the data flow. Process the data and transmit an XON to resume the transfer. Not all external devices understand XON/XOFF handshaking. Be sure to check your device.

When attempting to use a remote terminal from Applesoft, the output appear on one line of the terminal's screen. To avoid this problem, use the Communications Card Print routine on page 28 of the Communications Interface Card manual. If you are using DOS 3.2 or later you must modify this routine with a POKE 845,110 before saving it to disk.

Modifying the default parameter settings on the Communications card is described on page 27 of the Communications Interface Manual. But please note that the PR#s and IN#s commands do not initialize the interface, they only reset the I/O vectors. It's the first character through the interface that

loads the default parameters. So be sure to PRINT or INPUT at least one character before doing the POKEs.

Apple Tech Notes

Keywords: <None>

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This information is from the Apple Technical Information Library.

19960215 11:05:19.00

Tech Info Library Article Number: 1136