



Tech Info Library

Apple II Hardware: Errata in Apple II Reference Manual (2 of 2)

Page 104

The +12 and -5 volt levels are documented on page 92 as +11.8 and -5.2. The levels will vary from Apple to Apple.

Page 107

Pin 19, SYNC, is connected only on Apples manufactured for sales overseas.

Page 107

Pin 21, RDY, is pulled high with a 1000 ohm resistor to +5 volts.

Page 107

Pin 22, DMA, is held high by a 1000 ohm resistor to +5 volts. This signal will stop the 6502 clock. It should not be held low for more than two clock cycles or the 6502 internal registers may be lost.

Page 108

Pin 28, INT IN, is the second item on the page and is mislabeled 26.

Page 108

Pin 32, INH, is pulled high by a 1000 ohm resistor.

Page 108

Pin 35, COLOR REF, is connected only on Apples manufactured for sales overseas.

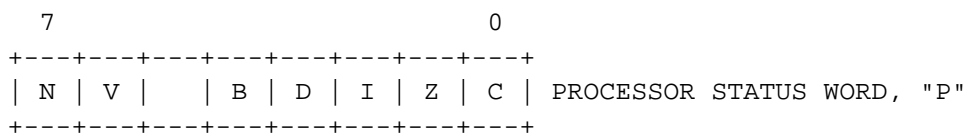
Page 119

Figure 3 should be labeled:

ROTATE ONE BIT RIGHT (MEMORY OR ACCUMULATOR) M or A.

Page 120

The Processor status word should be



^
This bit is undefined.

Page 121

Note 1 should read "Bits 6 and 7 are transferred to the Status Register. If

the result of A AND M is zero, then Z=1; otherwise Z=0."

Page 127-128

The unimplemented opcodes are shown as NOPs, which is wrong. \$EA is the only code defined as NOP. The others should not be used as they perform undefined operations.

Page 128

Op-code \$AD is a LDA, Absolute

Page 137

The addresses starting at line 100 should be:

```
CLRAN0 EQU $C058
SETAN0 EQU $C059
CLRAN1 EQU $C05A
SETAN1 EQU $C05B
CLRAN2 EQU $C05C
SETAN2 EQU $C05D
CLRAN3 EQU $C05E
SETAN3 EQU $C05F
```

Page 143

Starting at address \$FA6F the comments should read:

```
FA6F LDA CLRAN0 ;AN0 = TTL LO
FA72 LDA CLRAN1 ;AN1 = TTL LO
FA75 LDA SETAN2 ;AN2 = TTL HI
FA78 LDA SETAN3 ;AN3 = TTL HI
```

Page 165

The comment after address \$FCAC should read

```
1.0204 USEC * (13+27/2*A+5/2*A*A)
```

Pages 172-176

These tables were cut up to fit the pages so they are no longer in numeric or alphabetic order.

Apple Tech Notes

Keywords: <None>

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