Revision History

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
BT1	
C194	C37-42 C44-46 C133-134 C140-144
D2	
F2	
G2	G1
J18	
L14	L3-5 L10
LP3	
Q8	
R142	R17 R66-67 R71-74 R76-77 R89 R129
RP14	RP7
S1	
TP266	TP93-94 TP99-100 TP102-103 TP106 TP111-112 TP115-117 TP119-125 TP127-129 TP166 TP175 TP189-190 TP194 TP198 TP217-218 TP220-221 TP255 TP259
U35	U12-15 U31 U34
Y2	Y1

Proto2 to EVT1	
Page 2	Added R95, R96 to route BCLK/2 to SCSI_CLK for 33 MHz board Rearranged signals on RP1 for ease of routing Changed U1 from 355S0002 to 359S0021 (MC88916 to MC88920) Changed R13 from 365Ω to 95.3Ω for 88920 Added R130, R131 to select 88920 or CUDA as Sys_Reset* source
Page3	Rearranged signals on RP3 for ease of routing
Page 4	Added R99 to pull up CUDA RESET* output
Page 5	Added U23, U25, C125, C126, R97, and R98 to put ROM on board
Page 7	Added U34 and R129 to expand CPU ID field to 8 bits
Page 8	Changed J5 from 519-0595 to 519-0591
Page 9	Changed J6 from 515-0180 to 515-0908
Page 10	Changed BClk2 to SCSI_CLK Added C121 and R94 as termination for SCSI_CLK Rearranged signals on RP14 for ease of routing Changed J8 from 519-0597 to 519-0593
Page 11	Changed J11 from 517-0541 to 517-0714 (snap in 8 pin DIN) Changed J10 from 517-0541 to 517-0764 (9 pin DIN) for WorldPort Added C123 to bypass +5VFF for WorldPort connector
Page 12	Changed J14 from 517-0542 to 517-0715
Page 13	Removed U31, R71-R74, R76, R77, and C140-C143 Added R100 and R101 to attenuate DFAC II speaker driver Added U33, R102-R127, C176-C185, Q3, and Q4 for sound output only option Added R128 for sound input ground isolation Added D2, Q5-Q7 to protect DFAC II from ESD
Page 14	Added test points

EVT1 to Validation	
Page 2	Changed R13 from 95.3Ω to 121Ω per 88920 4-corner testing
Page 3	Added U35 and R136 to drive SlotReset* with CPU_RSTO* Added C189-C194 to bypass I/O Expansion Slot
Page 4	Removed RP7, R89 (signal termination for VRAM bank 1)
Page 6	Removed U12-U15, C37-C42, C44-C46, R17 to remove onboard VRAM
Page 7	Changed R20 from 10Ω to 33Ω (101S1331) Changed R30, R93 from 0Ω to 47Ω (101S1471) Changed R31 from 4.7KΩ to 1.5KΩ (101S1153) Changed R32 from 1.8KΩ to 1KΩ (101S1103) Changed R92 from 5.6Ω to 3.3Ω (101S1330) Removed U34 and R129 (PrimeTime2 does the right thing) Added R132-R133, J18 to correctly set Primus/Aladdin CPU_ID bit 2
Page 8	Changed R41 from 22Ω to 47Ω (101S1471) Changed C73, C80, C82 from 100pF to 1000pF (131S1033) Removed L3-L5 Added R138-R139 to bridge digital and chassis grounds Added R140-R142 to create RC low pass filter for RGB outputs
Page 9	Added R137, C188 to filter BGACK*
Page 10	Changed J7 from 515-0843 to 515-0906
Page 12	Changed U29 (CUDA) from version 2.35 to version 2.37 (341S0788)
Page 13	Changed C149, C150 from 22µF to 47µF (126S4710) Changed J16 from 515-0431 to 519-0815 Changed J16 again (from 519-0815 to 515-0439) Changed R101 from 18KΩ to 1.5KΩ (101S1153) Changed R103, R112 from 750Ω to 6.2KΩ (101S1623) Changed R104, R113 from 510Ω to 4.7KΩ (101S1473) Changed Q2 from 2N3906 to 2N3904 (372S3904) Removed R66, R67 Added R134-R135 and C186-C187 to sound output circuitry
Page 14	Changed TP62 connection from DSF0 to BGACKF* Moved TP62, TP151, TP176, TP256 Added TP260-TP266 Removed TP93-TP94, TP166, TP175, TP189-TP190, TP194, TP198, TP255

PRIMUS Logic Board Schematics

Brazil ROMs - 05

PRIMUS_VAL	Size: D	Rev	Build	Board	Date: 5/26/93
Table of Contents	Engineer: Jay Rickard				
© Apple Computer, Inc.	Page 1 of 14				

Note: For 33 MHz and 40 MHz machines, MC88920 must be replaced with MC88916, Apple part number 355S0002

Place Near MC68040

U2
68LC040-20

U1
MC88920

D[31:0] {4,5,7,8,9}
IPL*[2:0] {9}
IPL*[0] {3,7,9}
IPL*[1] {3,7,9}
IPL*[2] {3,7,9}
A[31:0] {3,4,5,8,9,10}
BG*_CPU {4}
BB* {3,4,9}
CDis*
MDis*
RW {3,4,8,9}
Snoop_Control[0]
Snoop_Control[1]
TT[0] {3}
TT[1] {3,4,9}
BS_CPUIN
BS_Mode*
TRst*
TEA* {4,9}
TA* {4,9}
TS* {4,9}
PClk
BS_Clk
Size[0] {3,4,9}
Size[1] {3,4,9}
TIP*_CPU {3}
LockE*
DLE*
MI* {4}
Lock* {3,4}
BR*_CPU {3,4}
TBI* {4,9}
CPU_RSTO* {3}
clkSync {7,14}
clkVcc {14}
clkEnable {14}
clkMR {14}
Reset* {4,12,14}
clkRC {14}
tpClkRC {14}
clkAGnd {14}
PLL_Reset* {14}
Sys_Reset* {3,9,13}
BClk1 {4}
BClk2 {9,14}
SCSI_CLK {10,14}
TCI040*
JSO
"JSO" for LC040

Stuff only one of R130 or R131

Stuff R96 only for 20 and 25 MHz boards
Stuff R95 only for 33 and 40 MHz boards

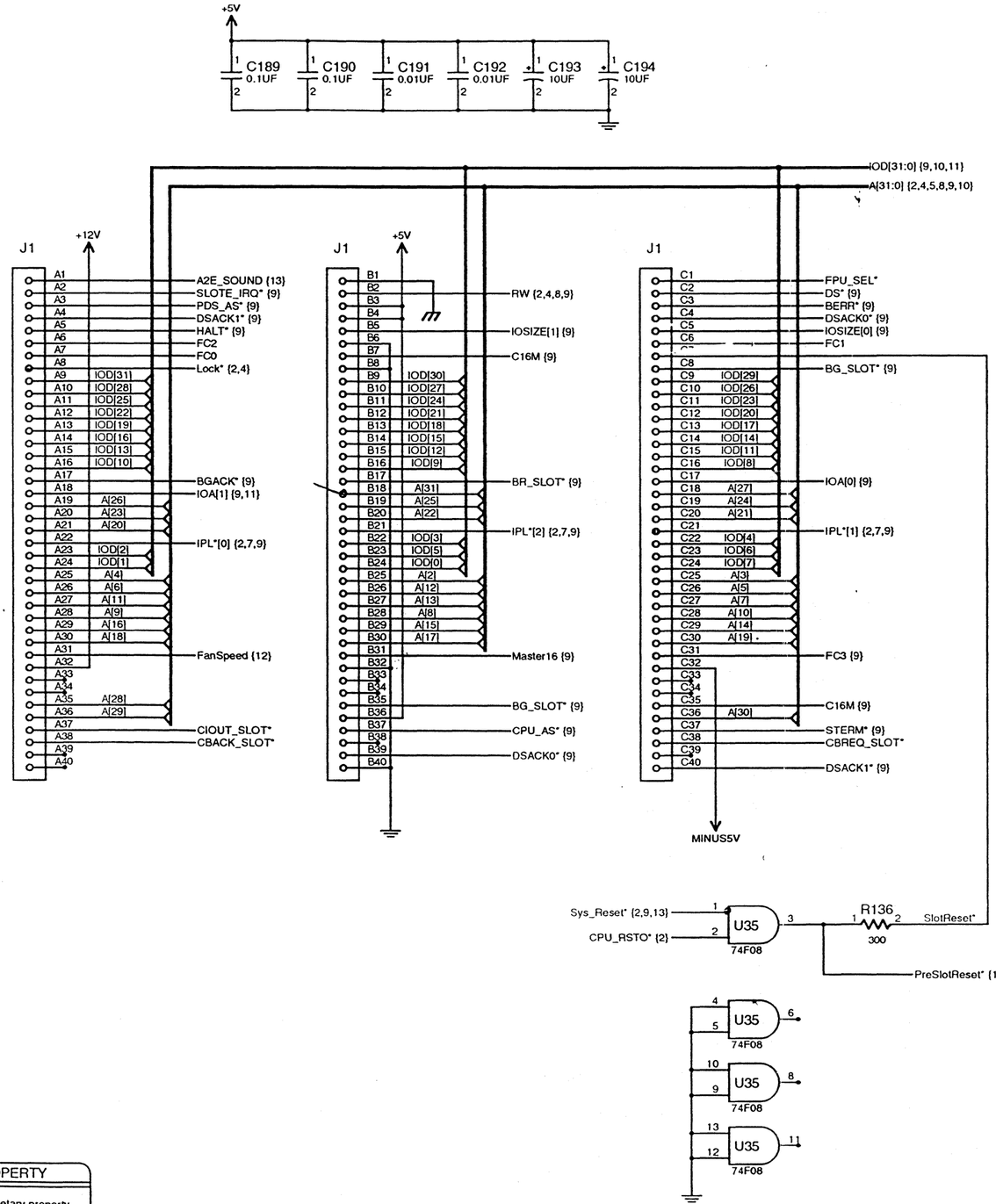
R13 varies with clock frequency	
20 MHz 106S1212, 1%, 121 ohm	
25 MHz 106S1212, 1%, 121 ohm	
33 MHz: 106S1402, 1%, 140 ohm	
40 MHz: 106S1102, 1%, 110 ohm	

Place These Termination at End of BClk Lines

PRIMUS_VAL
MC68040 and System Clock
Apple Computer, Inc.

Size	Rev	Build	Board	Date
D				4/22/93

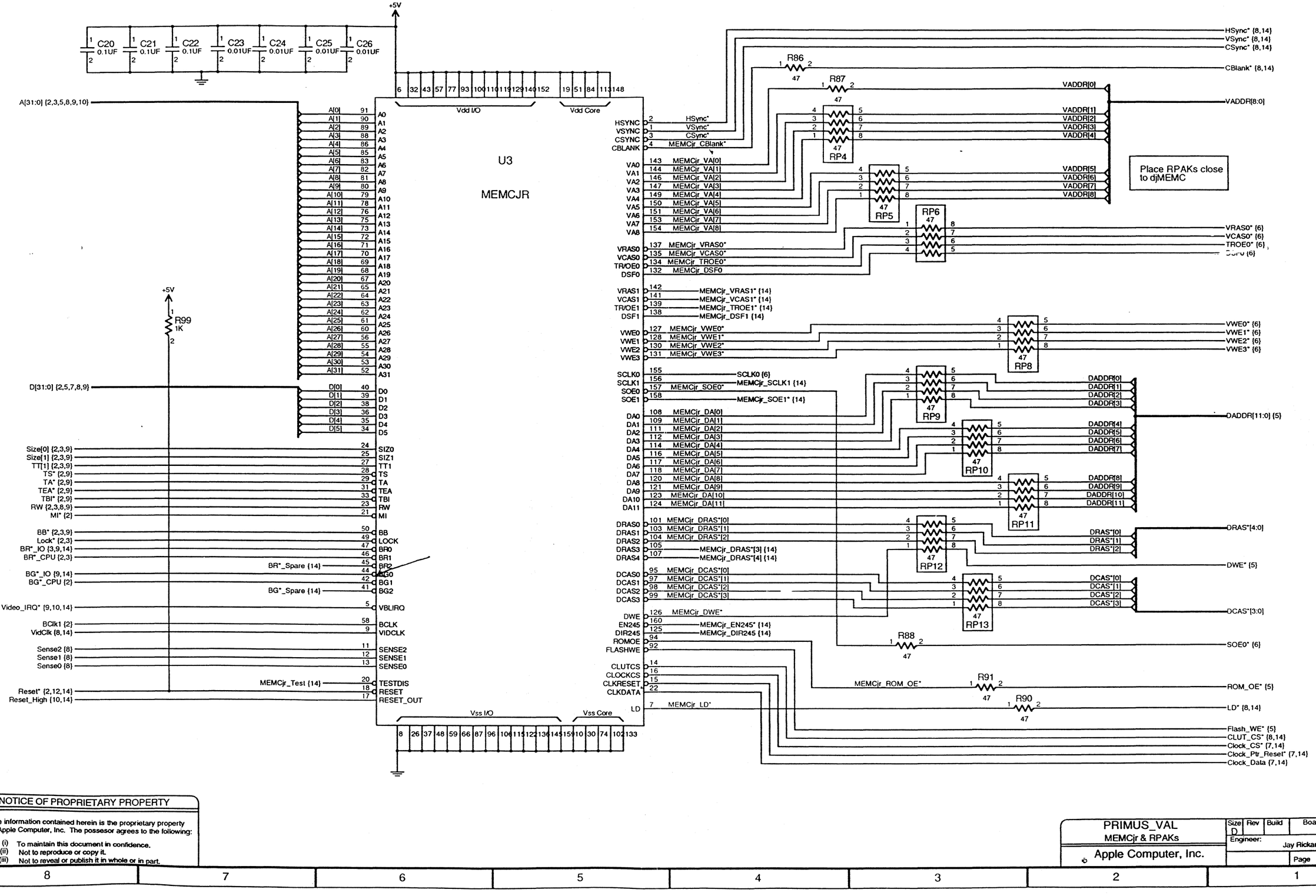
Engineer: Jay Rickard



PRIMUS_VAL
I/O Expansion Slot
Apple Computer, Inc.

Size	Rev	Build	Board	Date
D				4/19/93

Engineer: Jay Rickard



PRIMUS_VAL
MEMCjr & RPAKs
Apple Computer, Inc.

Size	Rev	Build	Board	Date
D				4/15/93

Engineer: Jay Rickard

D[31:0] {2,4,7,8,9}
DADDR[11:0] {4}

U4 DRAM-1MX4 — DADDR[0..9] — DWE* {4} — DRAS*[0] {4,14} — DCAS*[0] {4} — D[24] D[25] D[26] D[27]
U6 DRAM-1MX4 — DADDR[0..9] — DWE* {4} — DRAS*[0] {4,14} — DCAS*[1] {4} — D[16] D[17] D[18] D[19]
U8 DRAM-1MX4 — DADDR[0..9] — DWE* {4} — DRAS*[0] {4,14} — DCAS*[2] {4} — D[8] D[9] D[10] D[11]
U10 DRAM-1MX4 — DADDR[0] DADDR[1..8] DADDR[9] — DWE* {4} — DRAS*[0] {4,14} — DCAS*[3] {4} — D[0] D[1] D[2] D[3]
U5 DRAM-1MX4 — DADDR[0..9] — DWE* {4} — DRAS*[0] {4,14} — DCAS*[0] {4} — D[28] D[29] D[30] D[31]
U7 DRAM-1MX4 — DADDR[0..9] — DWE* {4} — DRAS*[0] {4,14} — DCAS*[1] {4} — D[20] D[21] D[22] D[23]
U9 DRAM-1MX4 — DADDR[0..9] — DWE* {4} — DRAS*[0] {4,14} — DCAS*[2] {4} — D[12] D[13] D[14] D[15]
U11 DRAM-1MX4 — DADDR[0..9] — DWE* {4} — DRAS*[0] {4,14} — DCAS*[3] {4} — D[4] D[5] D[6] D[7]

+5V

DRAM SIMM 1
J2

DRAS*[2] {4}
DRAS*[1] {4}
DCAS*[1] {4}
DCAS*[2] {4}
DCAS*[3] {4}
DCAS*[0] {4}
DWE* {4}

A[31:0] {2,3,4,8,9,10}
D[31:0] {2,4,7,8,9}

R98 4.7K

U23 ROM-256KX16 — A[2..19] — D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7] D[8] D[9] D[10] D[11] D[12] D[13] D[14] D[15]
U25 ROM-256KX16 — A[2..19] — D[16] D[17] D[18] D[19] D[20] D[21] D[22] D[23] D[24] D[25] D[26] D[27] D[28] D[29] D[30] D[31]

C125 0.1UF
C126 0.1UF

ROM_CE*
ROM_OE* {4}
ROM_BYTE {14}

R97 300

Flash_WE* {4}
ROM_OE* {4}

ROM SIMM
J3

ROM SIMM must have pin 11 connected to +5v
and the CE* on the ROM SIMM must be tied to GND

C35 47UF
C36 47UF

DRAM SIMM Bulk Bypass Caps
Place near DRAM SIMMs

DRAM Bypass Caps
C27 0.01UF
C29 0.01UF
C31 0.01UF
C33 0.01UF

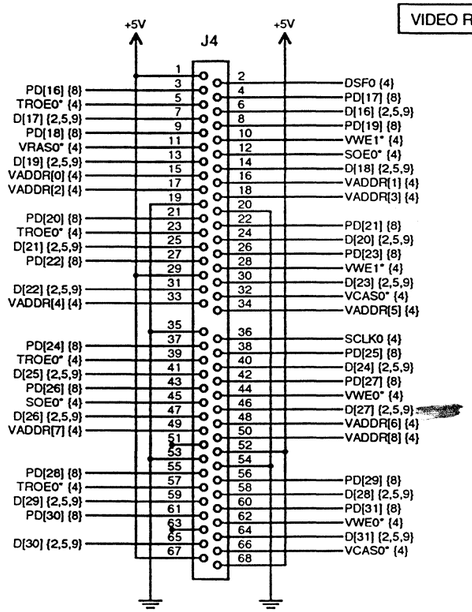
DRAM Bypass Caps
C28 0.01UF
C30 0.01UF
C32 0.01UF
C34 0.01UF

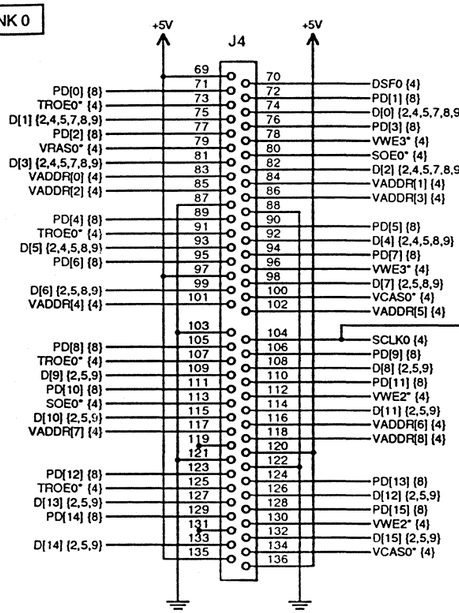
PRIMUS_VAL
DRAM (soldered), DRAM SIMM, & ROM SIMM
Apple Computer, Inc.

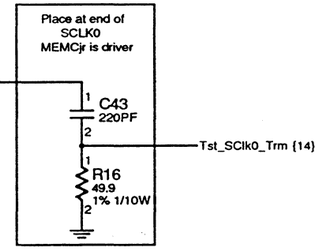
Size	Rev	Build	Board	Date
D				4/15/93

Engineer: Jay Rickard

VIDEO RAM BANK 0



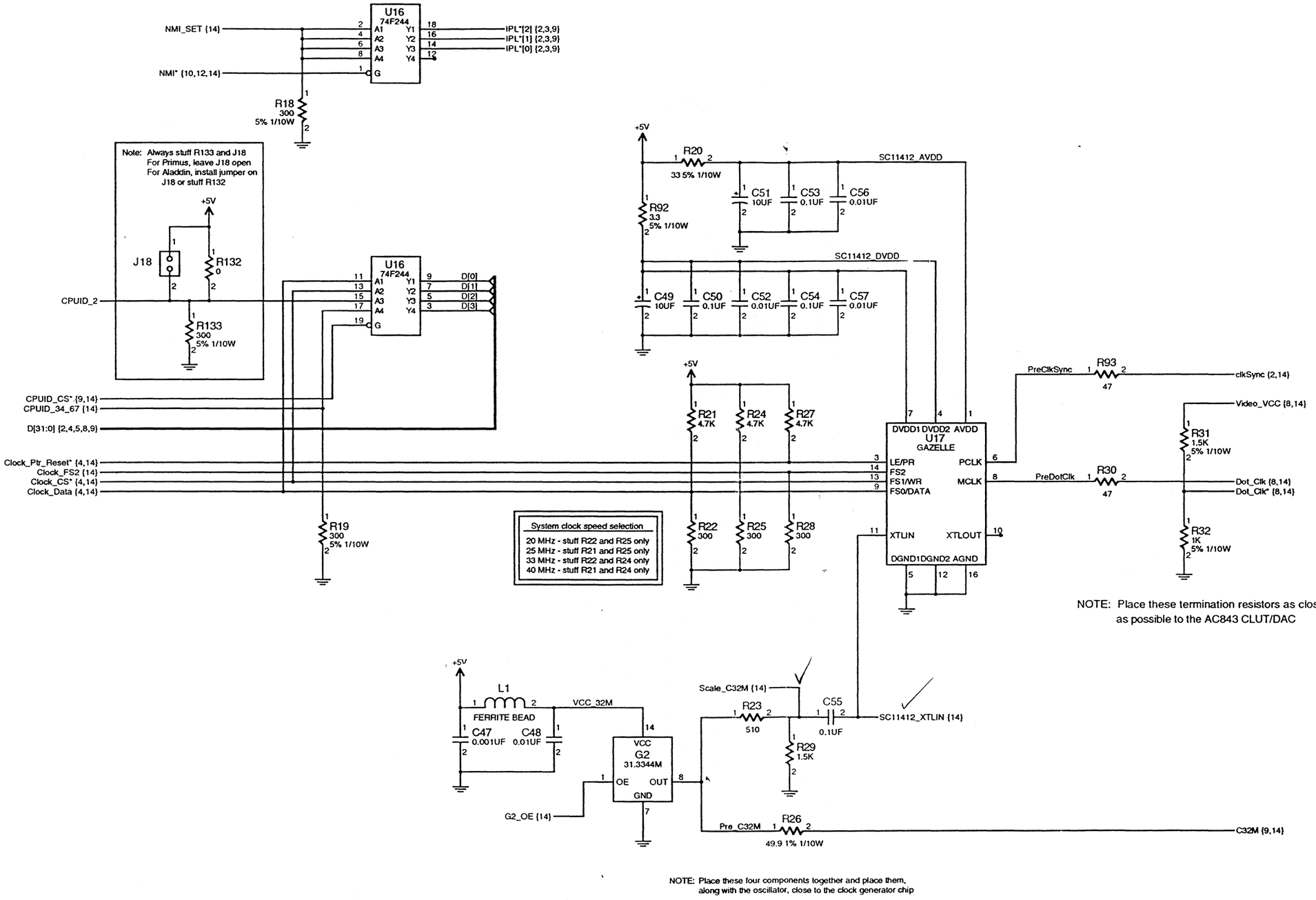




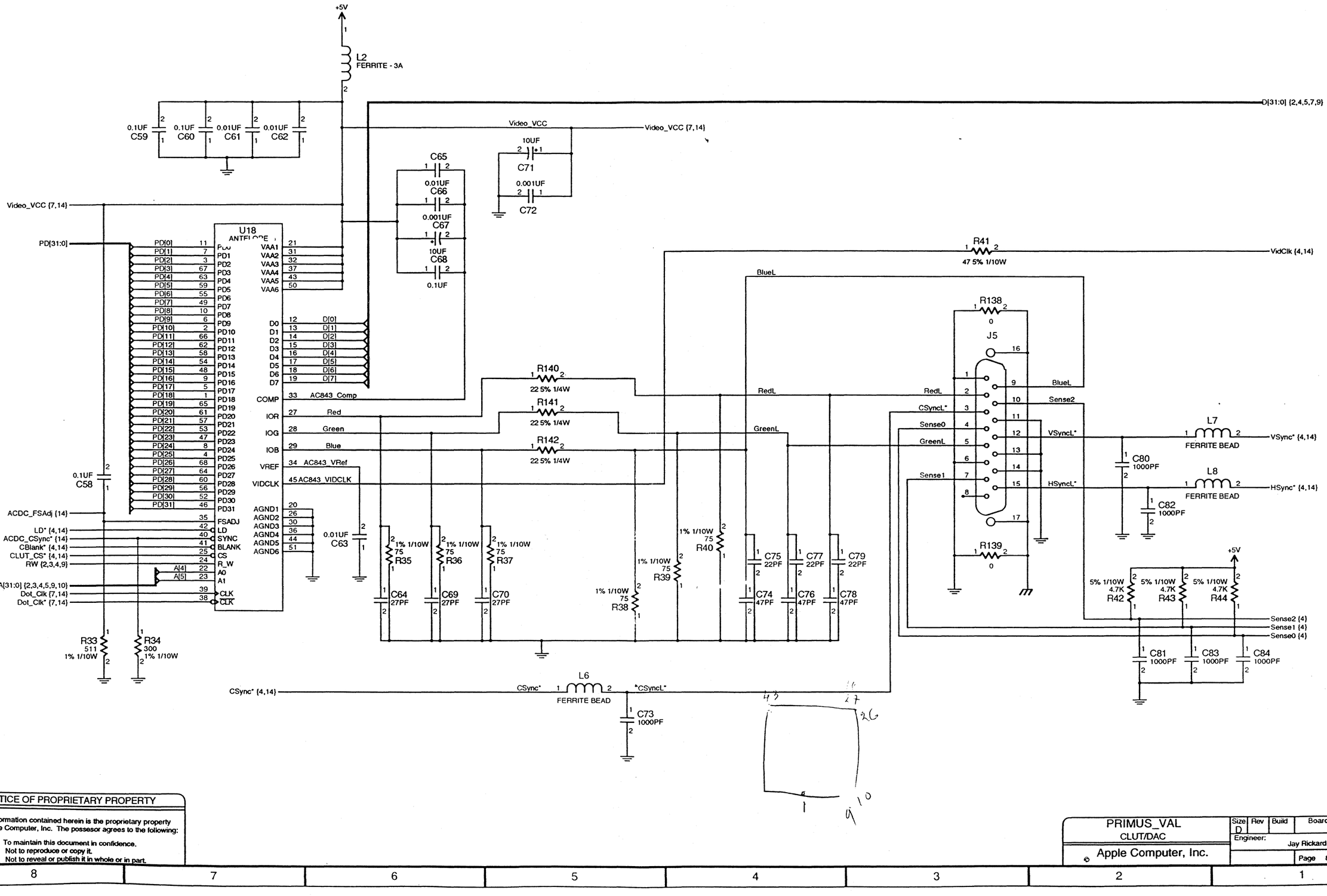
PRIMUS_VAL
VRAM SIMMs
Apple Computer, Inc.

Size	Rev	Build	Board	Date
D				4/15/93

Engineer: Jay Rickard



PRIMUS_VAL	Size: D	Rev	Build	Board	Date: 5/26/93
Video Clock Generator	Engineer: Jay Rickard				
© Apple Computer, Inc.				Page 7 of 14	

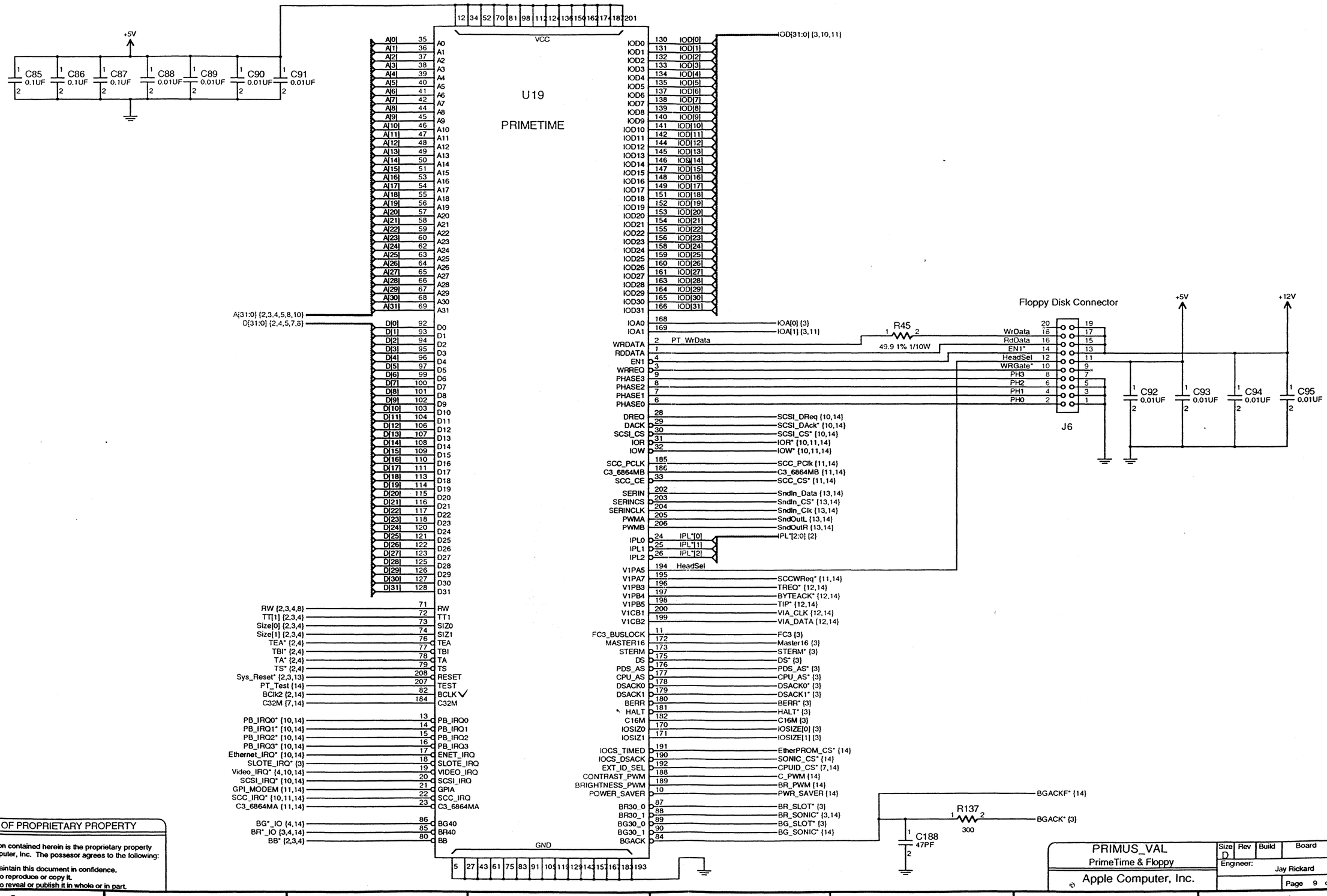


PRIMUS_VAL
CLUT/DAC

© Apple Computer, Inc.

Size	Rev	Build	Board	Date
D				4/29/93

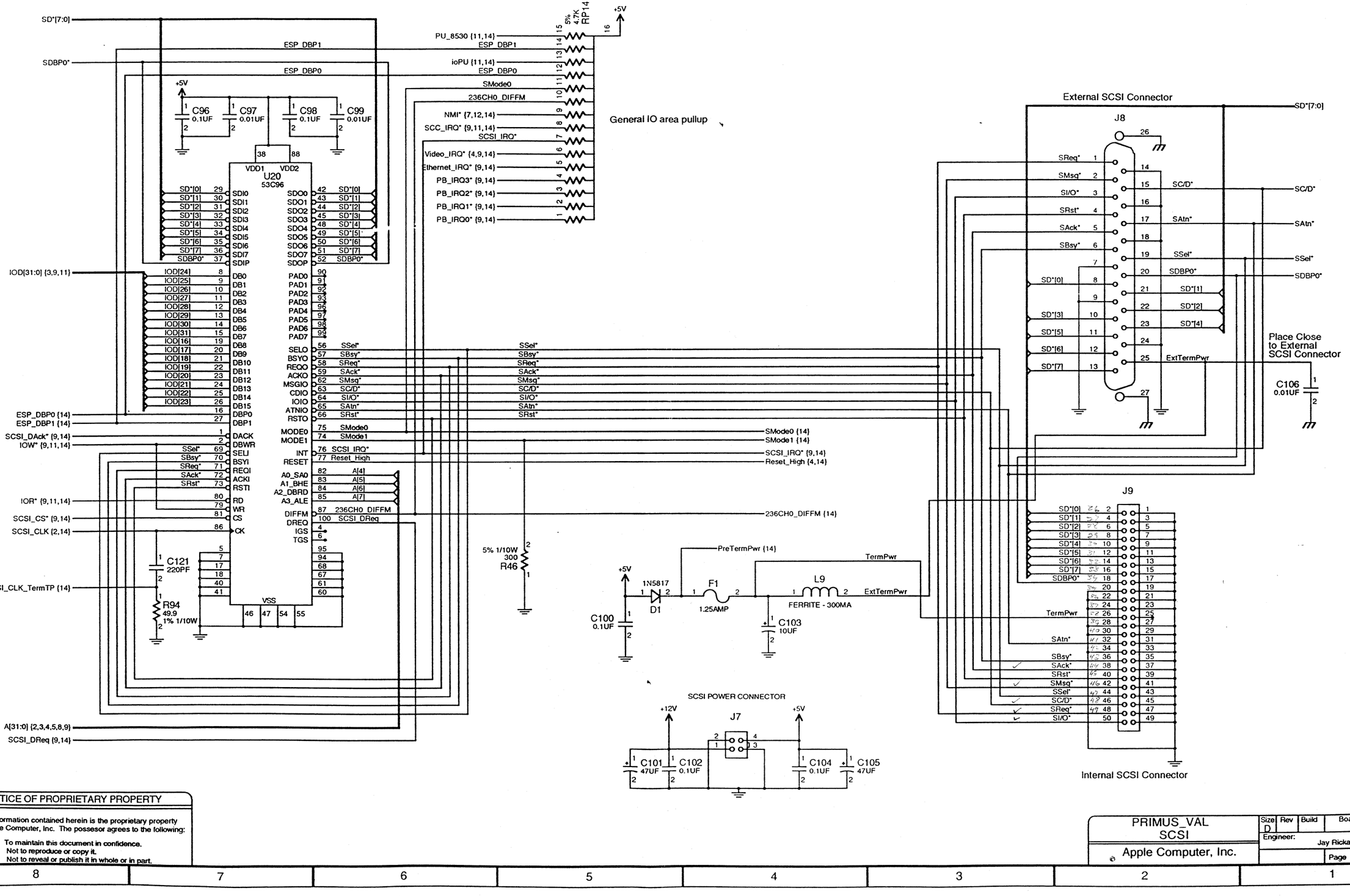
Engineer: Jay Rickard



PRIMUS_VAL
PrimeTime & Floppy
Apple Computer, Inc.

Size	Rev	Build	Board	Date
D				5/7/93

Engineer: Jay Rickard

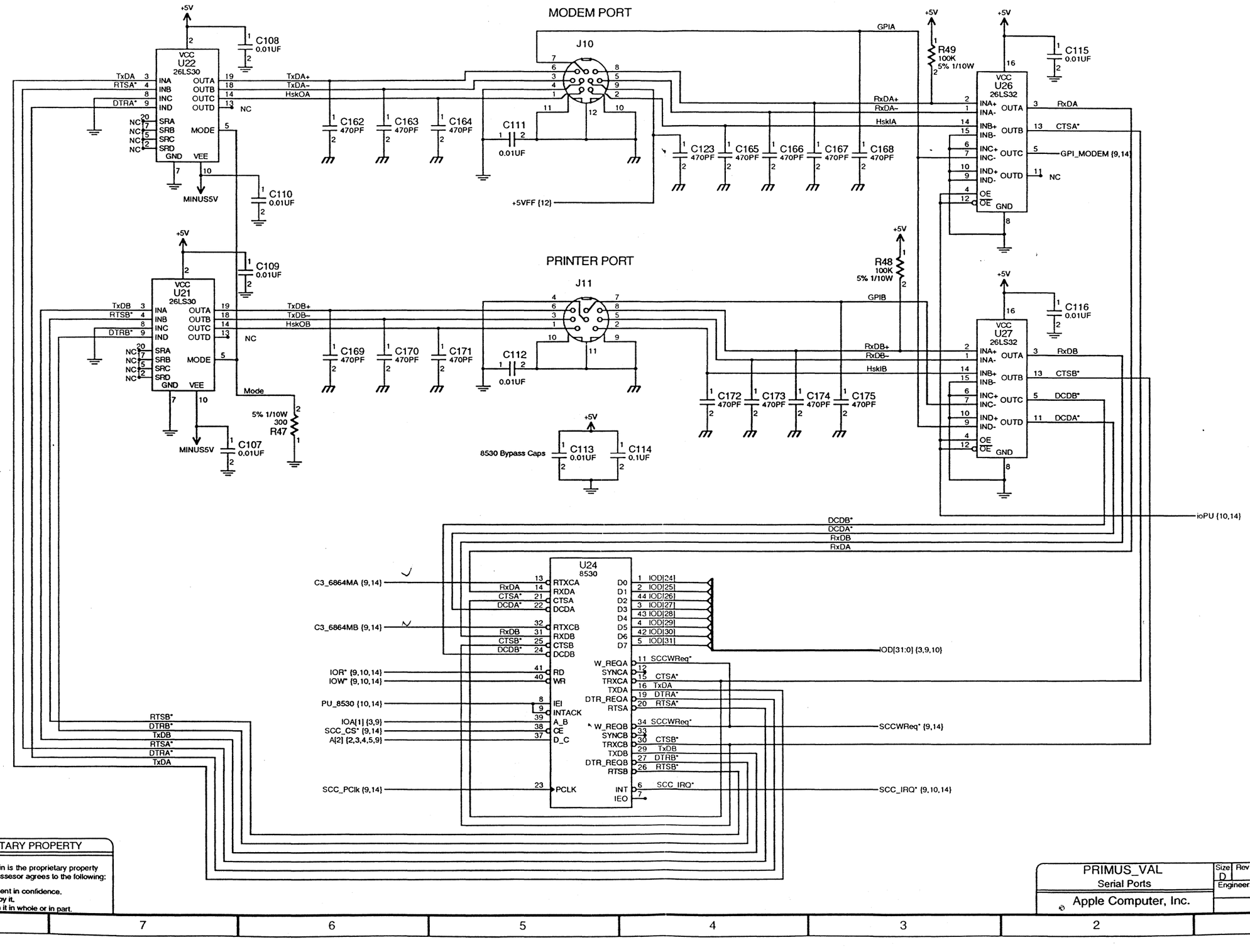


PRIMUS_VAL
SCSI

Apple Computer, Inc.

Size	Rev	Build	Board	Date
D				4/19/93

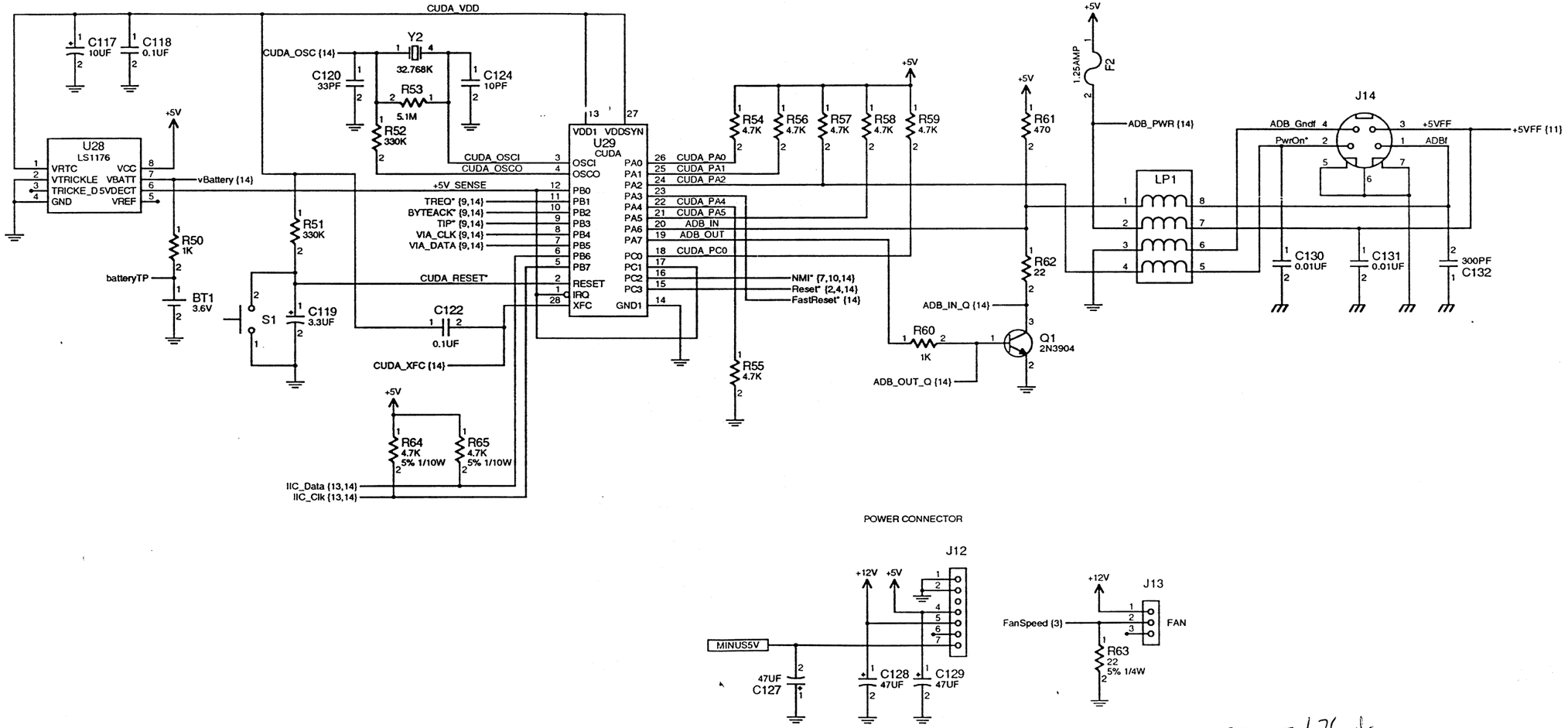
Engineer: Jay Rickard



PRIMUS_VAL
Serial Ports
Apple Computer, Inc.

Size	Rev	Build	Board	Date
D				4/15/93

Engineer: Jay Rickard



POWER CONNECTOR

60 mA × 22 Ω = 1.76 vdc

PRIMUS_VAL
CUDA, ADB Port, Power
Apple Computer, Inc.

Size D | Rev | Build | Board | Date 4/15/93
Engineer: Jay Rickard
Page 12 of 14

Note: The components in block #1 are needed only for a board that has sound output capability only (no sound input). See the BOM for the stuff/don't stuff component list.

1) Change R135 to 470kΩ
2) Change R134 to 0Ω
3) Remove R68
4) Short Q2-1 to Q2-3
   Remove Q2;3

#1

QVCC {14} R103 6.2K 5% C186 1uF 2 SndOutLD 1 R105 14.7K 1% 2 solL 1 R106 47.5K 1% 2 solL 2 R107 75K 1% 2 solL 3 R108 2.55K 1% mixL 3
SndOutLQ {14}
SndOutLB {14}
R102 10K 5%
Q3 2N3904
R104 4.7K 5%
C176 1500pF C177 1500pF C178 1500pF C179 1500pF C180 0.1UF
R122 200K 1% R123 200K 1% mixL* R124 100K 1%
QVCC {14} U33 TLE2062 V+ V- QVEE {14}
R109 75 1% R110 68.1 1%
SndOut_HPOL {14}
HPOL_ATT {14}

QVCC {14} R112 6.2K 5% C187 1uF 2 SndOutRD 1 R114 14.7K 1% 2 solR1 1 R115 47.5K 1% 2 solR2 1 R116 75K 1% 2 solR3 1 R117 2.55K 1% mixR 5
SndOutRQ {14}
SndOutRB {14}
R111 10K 5%
Q4 2N3904
R113 4.7K 5%
C181 1500pF C182 1500pF C183 1500pF C184 1500pF C185 0.1UF
R125 200K 1% R126 200K 1% mixR* R127 100K 1%
QVCC {14} U33 TLE2062 V+ V- QVEE {14}
R118 75 1% R119 68.1 1%
SndOut_HPOR {14}
HPOR_ATT {14}

R120 10K
R121 10K

QVCC {14} R135 750 470K C135 0.1UF
A2DC {14}
A2E_SND_IN {14}
A2E_SOUND {3} R134 10K 5%
Q2 2N3904
R68 510 R69 47K
A2B {14}
remove

SpkrDrv R100 47K 5% 1/10W
SpkerDrv* R81 47K 5% 1/10W

U30 DFAC-II

21	DVCC		
17	ATESTOUT	SPKR+	13
6	ATESTIN	SPKR-	14
26	SAMPCLK	ATTENL	10 AttenL
25	FADCLK	HPINL	11 hpInL
22	SCLK	ATTENR	9 AttenR
23	SDATA	HPINR	8 hpInR
24	RESET	HPOUTL	4 HPOL
28	EXPAND	OUTSENSE	7 OUT_SENSE
27	ADOUT	HPOUTR	3 HPOR
19	PWML	MICPWR	39 PRE_MIC_PWR
18	PWMR	UPGRADE	38 MIC_POWER
36	INTMIC	MICSENSE	37 MIC_SENSE
34	MODEMIN	LEFTIN	43 LEFT_IN
33	MODEMOUT	RIGHTIN	42 RIGHT_IN
35	MGND	INSENSE	40 IN_SENSE
44	QGND	SIGCOMMON	41 IN_COMMON
2	HPVCC	BYPASS	32
1	QVCC	VREF+	31
12	SPKRVCC	VREF-	30
6	QVEE	DGND	20 29
5	HPVEE		
15	SPKRVEE		

C151 C147 C152 C148 3.3UF
hpInL_TP {14}
hpInR_TP {14}
HPOL 3.3UF

SndIn_CS* {9,14}
SndIn_Clk {9,14}
IIC_Clk {12,14}
IIC_Data {12,14}
Sys_Reset* {2,3,9}
SndIn_Data {9,14}
SndOutL {9,14}
SndOutR {9,14}

R70 47K ModemIn ModemOut

+5V L11 100UH QVCC
C136 100UF C138 0.1UF
L12 100UH QVEE
C137 100UF C139 0.1UF
D2 1N5817
MINUS5V

C145 0.1UF C146 0.1UF C149 47UF C150 47UF
BypassTP {14}
BYPASS {14}
VREF+ {14}
VREF* {14}

Bridge1 {14} R75 1 1% 1/10W L13 FERRITE BEAD

R79 33 5% 1/10W R80 33 5% 1/10W
HPOR_ATT OUT_SENSE HPOL_ATT
LP3
HPOR_ATTF OUT_SENSEF SndOutOnlyL HPOL_ATTF
J16 Sound Out Jack
C158 0.001UF C160 0.001UF
Q5 Q7 2N3904 2N3904
Q6 Q8 2N3904 2N3904
HPOL_Prot {14}
HPOR_Prot {14}

+12V
FERRITE BEAD L14
C154 0.1UF
C153 0.1UF
+12VSound {14}
R85 6.8 5% 1W
Spkr_Amp_Pwr2 {14}
C161 10UF
Spkr_Amp_In {14}
SpkrAD {14}
C155 0.1UF
R83 27K 5% 1/10W
U32 TDA7052AT VP IN+ VC O+ O- N.C. GND
Spkr_Out+
Spkr_Out-
J17
Spkr_Amp_Vol {14}
R101 1.5K 5% 1/10W
R84 4.7K 5% 1/10W

R82 100 5% 1/10W
R128 0
C156 0.001UF C157 0.001UF C159 0.001UF
LP2
UPGRADEF LEFT_INF RIGHT_INF SHIELD
J15 Sound In Jack
N.C.

PRIMUS_VAL
Sound Input & Sound Output
Apple Computer, Inc.

Size	Rev	Build	Board	Date
D				5/3/93

Engineer: Jay Rickard

+12VSound {13} — TP1
G2_OE {7} — TP2
+5V_SENSE {12} — TP3
236CH0_DIFFM {10} — TP4
2X_Clk {2} — TP5
A2DC {13} — TP6
A2E_SND_IN {13} — TP7
A2B {13} — TP8
AC843_Comp {8} — TP9
AC843_VIDCLK {8} — TP10
AC843_VRef {8} — TP11
ACDC_CSync* {8} — TP12
ACDC_FSAdj {8} — TP13
ADB_IN {12} — TP14
ADB_IN_Q {12} — TP15
ADB_OUT {12} — TP16
ADB_OUT_Q {12} — TP17
ADB_PWR {12} — TP18
AttenL {13} — TP19
AttenR {13} — TP20
BClk1TermTP {2} — TP21
BClk2TermTP {2} — TP22
BClk0 {2} — TP23
BClk2 {2,9} — TP24
BClkDiv2 {2} — TP25
BG*_IO {4,9} — TP26
BR*_IO {3,4,9} — TP27
BR_SONIC* {3,9} — TP28
BYPASS {13} — TP29
BYTEACK* {9,12} — TP30
Blue {8} — TP31
Bridge1 {13} — TP32
BypassTP {13} — TP33
C32M {7,9} — TP34
C3_6864MA {9,11} — TP35
C3_6864MB {9,11} — TP36
CBlank* {4,8} — TP37
CLUT_CS* {4,8} — TP38
CPUID_34_67 {7} — TP39
CPUID_CS* {7,9} — TP40
CSync* {4,8} — TP41
CTSA* {11} — TP42
CTSB* {11} — TP43
CUDA_OSC {12} — TP44

CUDA_OSCI {12} — TP45
CUDA_OSCO {12} — TP46
CUDA_PA0 {12} — TP47
CUDA_PA1 {12} — TP48
CUDA_PA2 {12} — TP49
CUDA_PA4 {12} — TP50
CUDA_PA5 {12} — TP51
CUDA_PC0 {12} — TP52
CUDA_VDD {12} — TP53
CUDA_XFC {12} — TP54
Clock_CS* {4,7} — TP55
Clock_Data {4,7} — TP56
Clock_FS2 {7} — TP57
Clock_Ptr_Reset* {4,7} — TP58
DCDA* {11} — TP59
DCDB* {11} — TP60
DRAS*[0] {4,5} — TP61
BGACKF* {9} — TP62
DTRA* {11} — TP63
DTRB* {11} — TP64
Dot_Clk {7,8} — TP65
Dot_Clk* {7,8} — TP66
ESP_DBP0 {10} — TP67
ESP_DBP1 {10} — TP68
Ethernet_IRQ* {9,10} — TP69
GPI_MODEM {9,11} — TP70
Green {8} — TP71
HPOL {13} — TP72
HPOL_ATT {13} — TP73
HPOR {13} — TP74
HPOR_ATT {13} — TP75
HSync* {4,8} — TP76
IIC_Clk {12,13} — TP77
IIC_Data {12,13} — TP78
IN_COMMON {13} — TP79
IOR* {9,10,11} — TP80
IOW* {9,10,11} — TP81
LD* {4,8} — TP82
LEFT_IN {13} — TP83
MEMCjr_CBlank* {4} — TP84
MEMCjr_DA[0] {4} — TP85
MEMCjr_DA[4] {4} — TP91
MEMCjr_DA[8] {4} — TP95
MEMCjr_DCAS*[0] {4} — TP97

MEMCjr_DRAS*[0] {4} — TP101
MEMCjr_DSF0 {4} — TP104
MEMCjr_DSF1 {4} — TP105
MEMCjr_LD* {4} — TP107
MEMCjr_ROM_OE* {4} — TP108
MEMCjr_SOE0* {4} — TP109
MEMCjr_SOE1* {4} — TP110
MEMCjr_VA[0] {4} — TP113
MEMCjr_VA[1] {4} — TP114
MEMCjr_VA[5] {4} — TP118
MEMCjr_VWE0* {4} — TP126
MIC_POWER {13} — TP130
Mode {11} — TP131
ModemIn {13} — TP132
ModemOut {13} — TP133
NMI* {7,10,12} — TP134
NMI_SET {7} — TP135
OUT_SENSE {13} — TP136
PB_IRQ0* {9,10} — TP137
PB_IRQ1* {9,10} — TP138
PB_IRQ2* {9,10} — TP139
PB_IRQ3* {9,10} — TP140
PRE_MIC_PWR {13} — TP141
PT_WrData {9} — TP142
PU_8530 {10,11} — TP143
PreClkSync {7} — TP144
PreDotClk {7} — TP145
PreTermPwr {10} — TP146
Pre_C32M {7} — TP147
QVCC {13} — TP148
QVEE {13} — TP149
RIGHT_IN {13} — TP150
ROM_BYTE {5} — TP151
RTSA* {11} — TP152
RTSB* {11} — TP153
Red {8} — TP154
Reset* {2,4,12} — TP155
Reset_High {4,10} — TP156
RxDA {11} — TP157
RxDB {11} — TP158
SC11412_AVDD {7} — TP159
SC11412_DVDD {7} — TP160
SC11412_XTLIN {7} — TP161
SCCWReq* {9,11} — TP162

SCC_CS* {9,11} — TP163
SCC_IRQ* {9,10,11} — TP164
SCC_PClk {9,11} — TP165

SCSI_CLK {2,10} — TP167
SCSI_CLK_TermTP {10} — TP168
SCSI_CS* {9,10} — TP169
SCSI_DAck* {9,10} — TP170
SCSI_DReq {9,10} — TP171
SCSI_IRQ* {9,10} — TP172
SMode0 {10} — TP173
SMode1 {10} — TP174

Scale_C32M {7} — TP176
SndIn_CS* {9,13} — TP177
SndIn_Clk {9,13} — TP178
SndIn_Data {9,13} — TP179
SndOutL {9,13} — TP180
SndOutR {9,13} — TP181
SpkerDrv* {13} — TP182
SpkrDrv {13} — TP183
Spkr_Amp_In {13} — TP184
Spkr_Amp_Pwr2 {13} — TP185
Spkr_Amp_Vol {13} — TP186
TIP* {9,12} — TP187
TREQ* {9,12} — TP188

Tst_SClk0_Trm {6} — TP191
TxDA {11} — TP192
TxDB {11} — TP193

VCC_32M {7} — TP195
VIA_CLK {9,12} — TP196
VIA_DATA {9,12} — TP197

VREF* {13} — TP199
VREF+ {13} — TP200
VSync* {4,8} — TP201
VidClk {4,8} — TP202
Video_IRQ* {4,9,10} — TP203
Video_VCC {7,8} — TP204
clkAGnd {2} — TP205
clkEnable {2} — TP206

clkMR {2} — TP207
clkRC {2} — TP208
clkSync {2,7} — TP209
clkVcc {2} — TP210
hpInL {13} — TP211
hpInL_TP {13} — TP212
hpInR {13} — TP213
hpInR_TP {13} — TP214
ioPU {10,11} — TP215
mixL {13} — TP216
mixR {13} — TP219
tpClkRC {2} — TP222
vBattery {12} — TP223
MEMCjr_DRAS*[3] {4} — TP224
MEMCjr_DRAS*[4] {4} — TP225
MEMCjr_Test {4} — TP226
C_PWM {9} — TP227
BR_PWM {9} — TP228
PWR_SAVER {9} — TP229
PT_Test {9} — TP230
BG_SONIC* {9} — TP231
SONIC_CS* {9} — TP232
EtherPROM_CS* {9} — TP233
FastReset* {12} — TP234
BR*_Spare {4} — TP235
BG*_Spare {4} — TP236
MEMCjr_EN245* {4} — TP237
MEMCjr_DIR245 {4} — TP238
SpkrAD {13} — TP239
SndOutOnlyL {13} — TP240
SndOut_HPOR {13} — TP241
SndOut_HPOL {13} — TP242
SndOutLQ {13} — TP243
SndOutRQ {13} — TP244
mixL* {13} — TP245
mixR* {13} — TP246
soL1 {13} — TP247
soL2 {13} — TP248
soL3 {13} — TP249
soR1 {13} — TP250
soR2 {13} — TP251
soR3 {13} — TP252
SndOutLB {13} — TP253
SndOutRB {13} — TP254

HPOR_Prot {13} — TP256
HPOL_Prot {13} — TP257
PLL_Reset* {2} — TP258

+5V
TP87
TP88
TP90
TP98

TP86
TP89
TP92
TP96

MEMCjr_VRAS1* {4} — TP260
MEMCjr_VCAS1* {4} — TP261
MEMCjr_TROE1* {4} — TP262
MEMCjr_SCLK1 {4} — TP263
SndOutLD {13} — TP264
SndOutRD {13} — TP265
PreSlotReset* {3} — TP266

PRIMUS_VAL
Test Points
Apple Computer, Inc.

Size	Rev	Build	Board	Date
D				4/16/93

Engineer: Jay Rickard