Developer Note

Apple Logic Board Design LPX-40

Developer Note

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About This Note

This developer note describes the Apple Logic Board Design LPX-40. It is intended to help experienced Macintosh hardware and software developers design compatible products. If you are unfamiliar with Macintosh computers or would simply like more technical information, you may wish to read the related technical documents listed in the section "Supplemental Reference Documents."

Contents of This Note

The information is arranged in five chapters and an index.

- Chapter 1, "Introduction," gives a summary of the features of the Apple Logic Board Design LPX-40 and discusses issues related to compatibility with other Macintosh computer software and hardware.
- Chapter 2, "Architecture," describes the organization of the logic board. This chapter includes a block diagram and descriptions of the main components of the logic board.
- Chapter 3, "I/O Features," describes the built-in input/output (I/O) device interfaces and the external I/O ports. It also describes the built-in video support for external video monitors.
- Chapter 4, "Expansion Features," describes the expansion slots on the Apple Logic Board Design LPX-40. This chapter provides guidelines for designing cards for the I/O expansion slot and brief descriptions of the expansion modules for the other slots.
- Chapter 5, "MFM Floppy Disk Device Driver," gives the program interface for the system software and the driver that supports systems configured with an MFM internal floppy disk drive.

Supplemental Reference Documents

For a description of the version of the Mac OS that supports the Apple Logic Board Design LPX-40, developers should refer to Technote 1050.

Developers should have the relevant books of the *Inside Macintos*h series. You should also have *Designing PCI Cards and Drivers for Power Macintosh Computers*. These books are available in technical bookstores and through the *Apple Developer Catalog*. You should also have the *ATA Device Software Guide* if you plan to develop software utilities or drivers for ATA or ATAPI devices.

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Conventions and Abbreviations

This developer note uses the following typographical conventions and abbreviations.

Typographical Conventions

New terms appear in **boldface** where they are first defined.

Computer-language text—any text that is literally the same as it appears in computer input or output—appears in `Courier` font.

Hexadecimal numbers are preceded by a dollar sign ($). For example, the hexadecimal equivalent of decimal 16 is written as $10.

Note
A note like this contains information that is interesting but not essential for an understanding of the text. ◆

IMPORTANT
A note like this contains important information that you should read before proceeding. ▲

Standard Abbreviations

When unusual abbreviations appear in this book, the corresponding terms are also spelled out. Standard units of measure and other widely used abbreviations are not spelled out. Here are the standard units of measure used in this developer note:

A	amperes	mA	milliamperes
dB	decibels	µA	microamperes
GB	gigabytes	MB	megabytes
Hz	hertz	MHz	megahertz
in.	inches	mm	millimeters
k	1000	ms	milliseconds
K	1024	µs	microseconds
KB	kilobytes	ns	nanoseconds
kg	kilograms	Ω	ohms
kHz	kilohertz	sec.	seconds
kΩ	kilohms	V	volts
lb.	pounds	W	watts

Here are other abbreviations that may used in this developer note:

$*n*	hexadecimal value *n*
AC	alternating current
ADB	Apple Desktop Bus
AV	audiovisual
AWACS	audio waveform amplifier and converter for sound
CD-ROM	compact disk read-only memory

CLUT	color lookup table
DAC	digital to analog converter
DAV	digital audio video
DDC	display data channel
DESC	digital video decoder and scaler
DIMM	dual inline memory module
DMA	dynamic memory access
DRAM	dynamic random-access memory
DVA	digital video application
EMI	electromagnetic interference
FPU	floating-point unit
GCR	group code recording
GIMO	graphic internal monitor out (for PC compatibility cards)
IC	integrated circuit
IDE	integrated device electronics
IIC	inter-integrated circuit (an internal control bus)
I/O	input/output
IR	infrared
LS TTL	low-power Schottky TTL (a standard type of device)
MESH	Macintosh enhanced SCSI hardware
MFM	modified frequency modulation
MMU	memory management unit
MOS	metal-oxide semiconductor
NTSC	National Television Standards Committee (the standard system used for broadcast TV in North America and Japan)
NMI	nonmaskable interrupt
PAL	Phase Alternating Line system (the standard for broadcast TV in most of Europe, Africa, South America, and southern Asia)
PCI	Peripheral Component Interconnect
PDS	processor-direct slot
PLL	phase locked loop
PWM	pulse-width modulation
RAM	random-access memory
RGB	a video signal format with separate red, green, and blue components
RISC	reduced instruction set computing
RMS	root-mean-square
ROM	read-only memory
SANE	Standard Apple Numerics Environment

SCSI	Small Computer System Interface
SCC	serial communications controller
SECAM	the standard system used for broadcast TV in France and the former Soviet countries
SIMM	single inline memory module
S-video	a type of video connector that keeps luminance and chrominance separate; also called a Y/C connector
SWIM	Super Woz Integrated Machine, a custom IC that controls the floppy disk interface
TTL	transistor-transistor logic (a standard type of device)
VCR	video-cassette recorder
VLSI	very large scale integration
VRAM	video RAM; used for display buffers
Y/C	a type of video connector that keeps luminance and chrominance separate; also called an S-video connector
YUV	a video signal format with separate luminance and chrominance components

CHAPTER 1

Introduction

The Apple Logic Board Design LPX-40 is a new Power Macintosh logic board that incorporates either a PowerPC™ 603e or PowerPC 604e microprocessor, a second-level (L2) cache expansion slot, three DRAM expansion slots, three or five Peripheral Component Interconnect (PCI) card expansion slots (with installation of a riser card), standard Macintosh I/O ports, two PS/2 serial ports to support a PS/2 keyboard and mouse, and support for an internal ATAPI CD-ROM drive. The Apple Logic Board Design LPX-40 layout follows the LPX form factor and can be housed in LPX low profile or tower enclosures.

Summary of Features

Here is a summary of the hardware features of the Apple Logic Board Design LPX-40. Each feature is described more fully later in this note.

- Microprocessor: PowerPC 603e microprocessor running at 160 MHz, 180 MHz, and 200 MHz, or PowerPC 604e microprocessor running at 160 MHz and 200 MHz.
- RAM: 0 MB soldered to the main logic board; expandable to 96 MB using 168-pin JEDEC-standard 3.3 volt unbuffered EDO (extended data out) DIMM (dual inline memory module) devices. Three DIMM slots are provided for DRAM expansion.
- ROM: 4 MB soldered on main logic board; 64-bit ROM data bus width.
- Cache: 256 KB L2 cache on a 160-pin DIMM card (optional).
- Macintosh standard 15-pin monitor connector or a 15-pin SVGA connector.
- Video display modes: the LPX-40 logic board provides support for a wide range of displays depending on the amount of video RAM installed. For a complete description of the display modes and pixel resolutions supported by the LPX-40 logic board, see “Built-in Video” beginning on page 38.
- 2D built-in graphics acceleration.
- Sound: 16 bits/channel stereo sound input and output, external rear jack for sound in, rear jack for headphones or amplified stereophonic speakers, and one built-in speaker.
- Hard disks: one internal 3.5-inch IDE hard disk with 1.2 GB or larger capacity; external SCSI port (DB-25) for additional SCSI devices. PIO, singleword DMA, and multiword DMA data transfers are supported.
- CD-ROM drive support: internal 8X-speed ATAPI CD-ROM drive.
- PCI card expansion slots: accepts either three or five 7-inch or 12-inch PCI cards depending on the enclosure and expansion/riser card configuration; available power for the slots is dependent on the enclosure power supply.
- Floppy disk support: one internal 1.4 MB Apple SuperDrive or one internal MFM floppy drive.
- Processor bus: 64-bit wide, 40 MHz, supporting split address and data tenures.
- Standard Macintosh I/O ports: two GeoPort serial ports, sound input and output jacks, a SCSI port, and an ADB port.

- PC standard I/O ports: two PS/2 serial ports for keyboard and mouse.
- Apple GeoPort: supported on the Macintosh printer and modem serial ports.
- Power switch: support for soft power from keyboard and power switch.
- Voltage switch: allows selection of either 115 for voltages of 100-130 V or 230 for voltages of 200-230 V depending on the voltage that you will be connecting to. The voltage selection must be set manually on the power supply.
- Energy saving: sleep, startup, and shutdown scheduling can be controlled with an Energy Saver control panel.

Comparison With Power Macintosh 6400 Computer

The LPX-40 main logic board is based on the architecture of the main logic board in the Power Macintosh 5400 and Macintosh Performa 6400 computers. Table 1-1 compares the features of the Apple Logic Board Design LPX-40 with the Macintosh Performa 6400 computer.

Table 1-1 Comparison with the Macintosh Performa 6400 series computer

Features	Macintosh Performa 6400	Apple Logic Board Design LPX-40
Processor type	PowerPC 603e	PowerPC 603e or 604e
Processor speed	120 MHz, 160 MHz, 180 MHz, 200 MHz	160 MHz, 180 MHz, and 200 MHz
Cache	256 KB L2 cache (optional)	256 KB L2 cache (optional)
Amount of RAM	8 MB–136 MB	0 MB–96 MB
RAM expansion	2 168-pin 5 volt fast-paged mode DIMMs	3 168-pin 3.3 volt unbuffered EDO DIMMs
Memory bus	64 bits, 40 MHz	64 bits, 40 MHz
Video RAM	1 MB (DRAM)	1 MB expandable to 4 MB (EDO DRAM, SDRAM, or SGRAM depending on logic board configuration)
Video input	Optional card for video input, capture, and overlay	None (third-party PCI cards)
Video output	Built-in video supports up to 1024-by-768 pixel resolution at 8 bits per pixel	Depending on the amount of video RAM installed, the built-in video supports up to 1280-by-1024 pixel resolution at 16 bits per pixel

continued

Table 1-1 Comparison with the Macintosh Performa 6400 series computer (continued)

Features	Macintosh Performa 6400	Apple Logic Board Design LPX-40
Graphics acceleration	None	2D graphics acceleration
Sound capabilities	8 or 16 bits/channel; stereo in, stereo record, stereo out; SRS surround-sound mode	8 or 16 bits/channel; stereo in, stereo record, stereo out
Remote control	Built-in IR receiver for optional TV/FM tuner card	None
Floppy disk drive	1, internal (GCR)	1, internal (MFM or GCR)
ADB ports	1	1
PS/2 ports	None	2, for PS/2 keyboard and mouse
Internal hard disk	1 (IDE/ATA)	Supports 1 (IDE/ATA)
Internal CD-ROM	1 SCSI	Supports 1 (ATAPI)
Internal SCSI expansion bay	1	None
External SCSI ports	1	1
Expansion slots	2 PCI slots for 7-inch cards	3 or 5 PCI slots for 7-inch or 12-inch PCI cards, depending on the riser card in the enclosure
DMA I/O	10 DMA channels	10 DMA channels
Serial ports	2, LocalTalk and GeoPort supported	2, LocalTalk and GeoPort supported

Compatibility Issues

The Apple Logic Board Design LPX-40 incorporates several changes from logic boards found in earlier desktop models. This section describes key issues you should be aware of to ensure that your hardware and software work properly with this new logic board. Some of the topics described here are covered in more detail in later parts of this developer note.

The gestalt values for the various Apple Logic Board Design LPX-40 configurations are listed in Table 1-2.

Table 1-2 Gestalt values for Apple Logic Board Design LPX-40 configurations

Gestalt value	Description of board configuration
511	Manual-eject MFM floppy drive with soft power
514	Auto-eject GCR floppy drive with soft power
516	Manual-eject MFM floppy drive with hard power
517	Auto-eject GCR floppy drive with hard power
518	Auto-eject MFM floppy drive with soft power
519	Auto-eject MFM floppy drive with hard power

MFM Floppy Drive

The Apple Logic Board Design LPX-40 has connectors for MFM (modified frequency modulation) and GCR (group code recording) floppy disk drives.

If the computer that the Apple Logic Board Design LPX-40 is installed in is equipped with an MFM floppy drive, Macintosh application copy protection schemes that rely on the GCR floppy drive, found in all previous Macintosh models, will no longer work with the MFM floppy. In addition, Macintosh disk drive utility programs should incorporate new code for manipulating data on the MFM floppy drive. For additional information about controlling the MFM floppy drive, see Chapter 5, “MFM Floppy Disk Device Driver.”

DRAM Expansion

The Apple Logic Board Design LPX-40 requires 168-pin 3.3 volt unbuffered EDO (extended data out) JEDEC-standard DRAM DIMM cards rather than the 168-pin 5 volt fast-page DIMM cards used in the Power Macintosh 5400, 7600, 8500, and 9500 computers and the Macintosh Performa 6400. The connector notches have different offsets to differentiate between device types and to ensure that the correct devices are installed on the logic board. For information about DRAM DIMM configurations supported on the Apple Logic Board Design LPX-40, see “DRAM DIMMs” beginning on page 48 in Chapter 4, “Expansion Features.”

The Apple Logic Board Design LPX-40 has three DRAM expansion slots. DRAM expansion slot 1 supports single-bank DIMMs. DRAM expansion slots 2 and 3 support both single-bank and dual-bank DIMMs. No DRAM is soldered on the main logic board.

DRAM DIMM developers should note that the PSX memory controller on the Apple Logic Board Design LPX-40 does not provide support for 4 M by 4 bits with 12-by-10 addressing, 1 M by 16 bits with 12-by-8 addressing, or with 11-by-9 addressing DRAM devices.

DRAM DIMM Dimensions

The JEDEC MO-161-B specification shows three possible heights for the 8-byte DIMM. For Macintosh computers, it is recommended that developers use only the shortest of the three: 1.100 inches. Taller DIMMs could put excessive pressure on the DIMM sockets due to possible mechanical interference inside the case.

Cache Expansion

The Apple Logic Board Design LPX-40 supports an optional 256K second-level DIMM cache card that includes an integrated cache controller. Apple does not support development of third-party cache cards for the Apple Logic Board Design LPX-40. The 160-pin cache expansion slot is the same as the cache slot found in the Power Macintosh 5400 and Macintosh Performa 6400 computer models.

ATA (IDE) Hard Disk and ATAPI CD-ROM Drive

The interface for the internal hard disk and CD-ROM drive on the Apple Logic Board Design LPX-40 is ATA (IDE) for the hard disk and ATAPI for the CD-ROM, not SCSI. This could cause compatibility problems for disk utility programs. The system software release for computers equipped with the Apple Logic Board Design LPX-40 includes version 3.0 or greater of the ATA Manager and supports PIO, singleword DMA, and multiword DMA data transfers. For more information about the software that controls ATA devices, see the *ATA Device Software Guide*.

PS/2 Keyboard Support

The Apple Logic Board Design LPX-40 provides two PS/2 serial ports for connection of a PS/2 keyboard and PS/2 mouse. The PS/2 implementation on the Apple Logic Board Design LPX-40 does not support all permutations of PS/2 keyboards and mouse devices. In particular, only two-button mouse devices are supported and only AT-type keyboards are supported.

The PS/2 to ADB conversion protocol, contained in the CudaLite ASIC, only supports PS/2 mouse devices that generate a binary 1 in the sync bit position (bit 3 of the first data byte) of the protocol. If the PS/2 mouse device generates a binary 0 in the sync bit position, the device is not recognized.

PC keyboards that implement XT or RT key codes are not supported. For additional information about PS/2 keyboard and mouse support on the Apple Logic Board Design LPX-40, see “PS/2 Keyboard and Mouse Ports” beginning on page 24.

Video Display RAM

In addition to 2D QuickDraw graphics acceleration, the Apple Logic Board Design LPX-40 has a new video RAM DIMM expansion implementation. It supports expansion of up to 4 MB of video RAM through a variety of video RAM devices. The Apple Logic

Board Design LPX-40 also supports DDC (display data channel) plug-and-play monitor identification.

For additional information about video display resolution and video display sense codes supported by the Apple Logic Board Design LPX-40, see “Built-in Video” on page 38. For a description of the new video RAM DIMM connector on the Apple Logic Board Design LPX-40, see “Video RAM” on page 58.

CHAPTER 2

Architecture

This chapter describes the architecture of the Apple Logic Board Design LPX-40. It describes the major components of the main logic board: the microprocessor, the custom ICs, and the display RAM.

Block Diagram and Main ICs

The Apple Logic Board Design LPX-40 can be configured with either the PowerPC 603e or PowerPC 604e microprocessor. The board is designed with many of the custom ICs that are used on the logic board in the Macintosh Performa 6400. Figure 2-1 shows the system block diagram. The architecture of the Apple Logic Board Design LPX-40 is based on two buses: the processor bus and the PCI bus. The processor bus connects the microprocessor, ROM, cache, and memory; the PCI bus connects the video expansion slots and the I/O devices.

Main Processor

The Apple Logic Board Design LPX-40 can be configured with either a PowerPC 603e or 604e main processor.

PowerPC 603e Microprocessor

The PowerPC 603e microprocessor runs at 160, 180, and 200 MHz. The principle features of the PowerPC 603e microprocessor include

- full RISC processing architecture
- parallel processing units: two integer and one floating-point
- a branch manager that can usually implement branches by reloading the incoming instruction queue without using any processing time
- an internal memory management unit (MMU)
- 32 KB of on-chip cache memory (16 KB for data and 16 KB for instructions)

For complete technical details, see the *PowerPC 603 RISC Microprocessor User's Manual.*

PowerPC 604e Microprocessor

The PowerPC 604e microprocessor runs at 160 and 200 MHz. The principle features of the PowerPC 604e microprocessor include

- full RISC processing architecture
- parallel processing units: load-store unit, two integer units, one complex integer unit, and one floating-point unit
- a branch manager that can usually implement branches by reloading the incoming instruction queue without using any processing time
- an internal memory management unit (MMU)

- 32 KB of on-chip cache memory (16 KB for data and 16 KB for instructions)

For complete technical details, see the *PowerPC 604 RISC Microprocessor User's Manual.*

Memory Subsystem

The memory subsystem of the Apple Logic Board Design LPX-40 consists of RAM, ROM, and an optional second-level (L2) cache. The PSX custom IC provides burst mode control to the cache and ROM.

RAM

There are no DRAM devices soldered on the logic board. Three slots are provided for RAM expansion. 168-pin 3.3 volt unbuffered EDO (extended data out) JEDEC-standard DRAM DIMM cards are required. The maximum supported DRAM is three slots containing 32 MB each for a total of 96 MB. For additional information about the supported DRAM devices, see "DRAM DIMMs" on page 48.

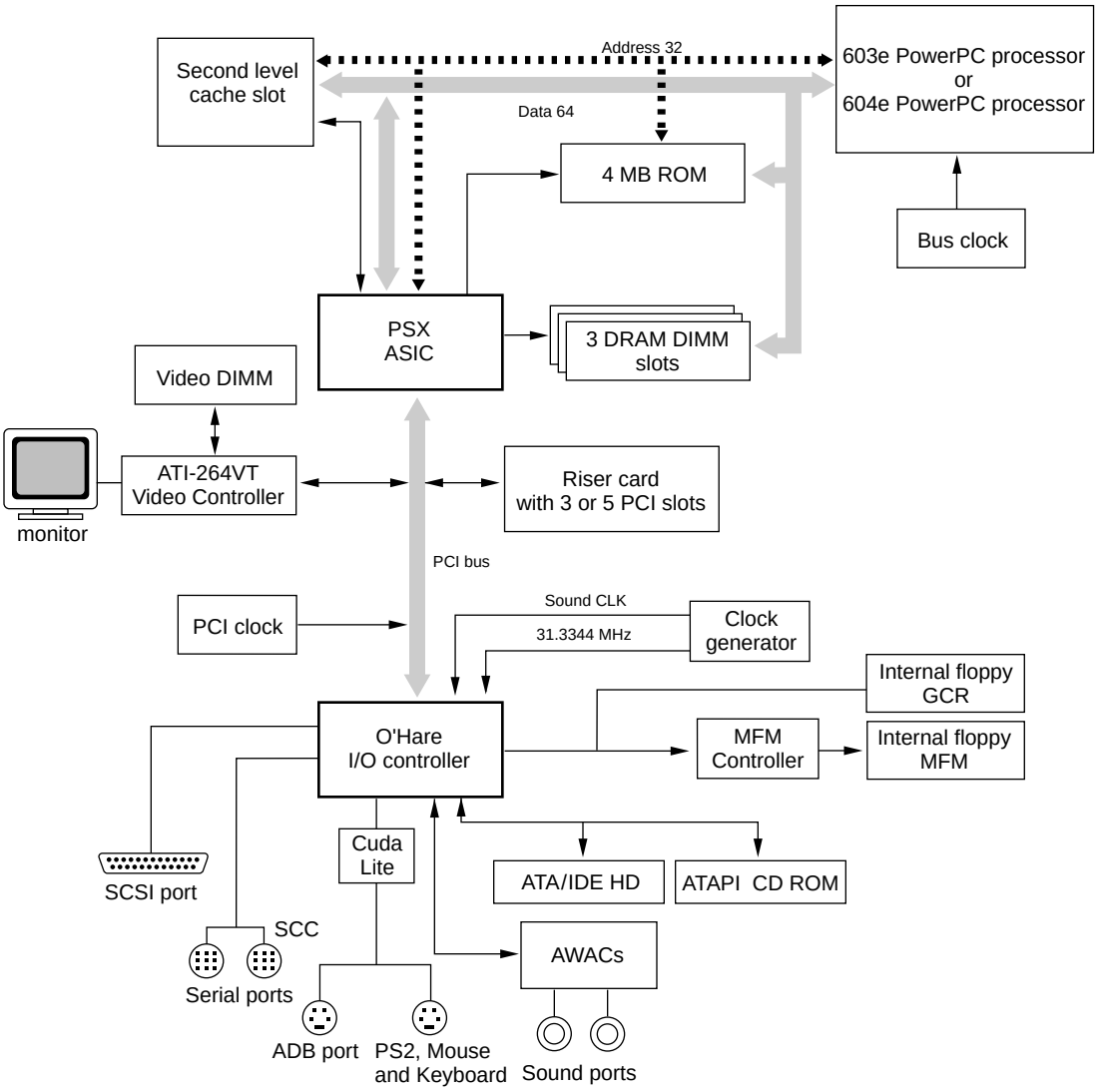
ROM

The ROM consists of 4 MB of masked ROM soldered to the main logic board.

Second-Level Cache (Optional)

The optional second-level (L2) cache consists of 256 KB of high-speed RAM on a 160-pin DIMM card, which is plugged into a 160-pin edge connector on the main logic board. For additional information about the second-level cache, see "Second-Level Cache DIMM" on page 56.

Figure 2-1 System block diagram



System RAM

The Apple Logic Board Design LPX-40 has no DRAM memory soldered on the main logic board. All RAM expansion is provided by 3.3 volt unbuffered EDO DRAM devices on 8-byte JEDEC-standard DIMMs. Three 168-pin DIMM sockets are used for memory expansion. Available DRAM DIMM sizes are 8, 16, and 32 MB. DIMM socket 1 supports one-bank DRAM modules. DIMM sockets 2 and 3 support both one- and two-bank DRAM modules. The PSX custom IC provides memory control for the system RAM. For additional information about supported DRAM, see "DRAM DIMMs" beginning on page 48.

Custom ICs

The architecture of the Apple Logic Board Design LPX-40 is designed around five large custom integrated circuits:

- the PSX memory controller and PCI bridge
- the O'Hare I/O subsystem and DMA engine
- the AWACS sound processor
- the CudaLite ADB controller
- the ATI 264VT-A4S2 graphics controller

The computer also uses several standard ICs that are used in other Macintosh computers. This section describes only the custom ICs.

PSX IC

The PSX IC functions as the bridge between the PowerPC 603e or the PowerPC 604e microprocessor and the PCI bus. It provides buffering and address translation from one bus to the other.

The PSX IC also provides the control and timing signals for system cache, ROM, and RAM. The memory control logic supports byte, word, long word, and burst accesses to the system memory. If an access is not aligned to the appropriate address boundary, PSX generates multiple data transfers on the bus.

Memory Control

The PSX IC controls the system RAM and ROM and provides address multiplexing and refresh signals for the DRAM devices. For information about the address multiplexing, see "RAM Address Multiplexing" on page 53.

PCI Bus Bridge

The PSX IC acts as a bridge between the processor bus and the PCI expansion bus, converting signals on one bus to the equivalent signals on the other bus. The PCI bridge functions are performed by two converters. One converter accepts requests from the

processor bus and presents them to the PCI bus. The other converter accepts requests from the PCI bus and provides access to the RAM and ROM on the processor bus.

The PCI bus bridge in the PSX IC runs asynchronously so that the processor bus and the PCI bus can operate at different rates. The processor bus operates at a clock rate of 40 MHz, and the PCI bus operates at 33.33 MHz.

The PCI bus bridge generates PCI parity as required by the PCI bus specification, but it does not check parity or respond to the parity error signal.

Big-Endian and Little-Endian Bus Addressing

Byte order for addressing on the processor bus is big endian and byte order on the PCI bus is little endian. The bus bridge performs the appropriate byte swapping and address transformations to translate between the two addressing conventions. For more information about the translations between big-endian and little-endian byte order, see Part One, "The PCI Bus," in *Designing PCI Cards and Drivers for Power Macintosh Computers.*

Processor Bus to PCI Bus Transactions

Transactions from the processor bus to the PCI bus can be either burst or nonburst. Burst transactions are always 32 bytes long and are aligned on cache-line or 8-byte boundaries. In burst transactions, all the bytes are significant. Burst transactions are used by the microprocessor to read and write large memory structures on PCI devices.

Note
For the processor to generate PCI burst transactions, the address space must be marked as cacheable. Refer to *Macintosh Technote Number 1008, Understanding PCI Bus Performance,* for details. ◆

Nonburst transactions can be of arbitrary length from 1 to 8 bytes and can have any alignment. Nonburst transactions are used by the processor to read and write small data structures on PCI bus devices.

PCI Bus to Processor Bus Transactions

For transactions from the PCI bus to the processor bus, the bridge responds only to PCI bus memory commands and configuration commands. On the processor bus, the bridge generates a burst transaction or a nonburst transaction depending on the type of command and the address alignment. For Memory Write and Invalidate commands that are aligned with the cache line, the bridge generates a burst-write transaction. Similarly, for Memory Read Line and Memory Read Multiple commands whose alignment is less than three-quarters through a cache line, the bridge generates a burst-read transaction. The maximum burst-read or burst-write transaction allowed by the bridge is 32 bytes—8 PCI beats.

Commands other than those mentioned here are limited to two beats if aligned to a processor bus doubleword boundary and to one beat otherwise.

O'Hare IC

The O'Hare IC is based on the Grand Central IC present in the Power Macintosh 7500 computer. It is an I/O controller and DMA engine for Power Macintosh computers using the PCI bus architecture. It provides power-management control functions for energy management features included on the Apple Logic Board Design LPX-40. The O'Hare IC is connected to the PCI bus and uses the 33.33 MHz PCI bus clock.

The O'Hare IC includes circuitry equivalent to the IDE, SCC, SCSI, sound, SWIM3, and VIA controller ICs. The functional blocks in the O'Hare IC include the following:

- support for descriptor-based DMA for I/O devices
- system-wide interrupt handling
- a SWIM3 floppy drive controller
- SCSI controller (MESH based)
- SCC serial I/O controller
- IDE hard disk interface controller
- sound control logic and buffers

The O'Hare IC provides bus interfaces for the following I/O devices:

- CudaLite ADB controller IC (VIA1 and VIA2 registers)
- AWACS sound input and output IC
- 8 KB nonvolatile RAM control

The SCSI controller in the O'Hare IC is a MESH controller. DMA channels in the O'Hare IC are used to support data transfers. The clock signal to the SCSI controller is 45.1584 MHz.

The O'Hare IC also contains the sound control logic and the sound input and output buffers. There are two DMA data buffers—one for sound input and one for sound output—so the computer can record sound input and process sound output simultaneously. The data buffer contains interleaved right and left channel data for support of stereo sound.

The SCC circuitry in the O'Hare IC is an 8-bit device. The PCLK signal to the SCC is a 15.6672 MHz clock (one half of the 33.3344 MHz reference frequency). The SCC circuitry supports GeoPort and LocalTalk protocols.

AWACS Sound IC

The audio waveform amplifier and converter (AWACS) is a custom IC that combines a waveform amplifier with a 16-bit digital sound encoder and decoder (codec). It conforms to the IT&T *ASCO 2300 Audio-Stereo Codec Specification* and furnishes high-quality sound input and output. For information about the operation of the AWACS IC, see Chapter 3 of *Developer Note: Power Macintosh Computers,* available on the developer CD-ROM and as part of *Macintosh Developer Note Number 8.*

CudaLite IC

The CudaLite IC is a custom version of the Motorola MC68HC05 microcontroller. It provides several system functions, including

- the ADB interface
- PS2 keyboard and mouse interface
- management of system resets
- management of the real-time clock
- on/off control of the power supply (soft power)

ATI 264VT-A4S2 IC

The ATI 264VT-A4S2 IC is a custom IC containing the logic for the video display. It includes the following functions:

- display memory controller, clock generator, and video DAC (digital-to-analog converter)
- video CLUT (color lookup table)
- 2D graphics acceleration
- true color palette DAC supporting pixel clock rates to 135 MHz for 1280-by-1024 resolution at 75 Hz
- hardware cursor up to 64x64x2
- DCC1 and DDC2B plug-and-play monitor support
- supports EDO DRAM up to 60 MHz memory clock across a 64-bit memory interface
- supports SDRAM or SGRAM up to 80 MHz memory clock, providing a bandwidth up to 640 MB per second

A separate data bus handles data transfers between the ATI 264VT-A4S2 IC and the display memory. The display memory data bus is 64 bits wide for display memory of 2 MB or greater. For 1 MB of display memory, the data bus is 32 bits wide. The ATI 264VT-A4S2 IC breaks each 64-bit data transfer into several pixels of the appropriate size for the current display mode—4, 8, 16, 24, or 32 bits per pixel.

The ATI 264VT-A4S2 IC has an internal phase locked loop (PLL) to generate clocks for the display memory interface and the pixel digital to analog converter (DAC).

The 2D graphics accelerator is a fixed-function accelerator for rectangle fill, line draw, polygon fill, panning/scrolling, bit masking, monochrome expansion, and scissoring with full ROP support.

Display RAM DIMM

The display memory is separate from the main memory. The Apple Logic Board Design LPX-40 supports +5 V EDO DRAM, +3.3 V SDRAM and +3.3 V SGRAM devices for

video memory expansion. The video memory DIMM can be configured as 1 MB, 2 MB, or 4 MB.

The maximum supported size for an EDO video DIMM is 2 MB. EDO video DIMMs larger than 2 MB provide no additional performance due to the limited bandwidth of the EDO devices.

With a 4 MB SGRAM DIMM, the display data generated by the computer can have pixel depths of 4, 8, 16, 24, or 32 bits for monitors up to 1024-by-768 pixels and 4, 8, or 16 bits for larger monitors up to 1280-by-1024 pixels.

For additional information about video on the Apple Logic Board Design LPX-40, see “Built-in Video” on page 38 and “Video RAM” on page 58.

CHAPTER 3

I/O Features

This chapter describes both the built-in I/O devices and the interfaces for external I/O devices. It also describes the types of external video monitors that can be used with the Apple Logic Board Design LPX-40.

Board Layout

The Apple Logic Board Design LPX-40 is built to the industry standard LPX 13-by-9 inch form factor and can be installed in many off-the-shelf low profile and tower enclosures. The layout of the connectors on the board is shown in Figure 3-1.

Figure 3-1 Apple Logic Board Design LPX-40 connector layout

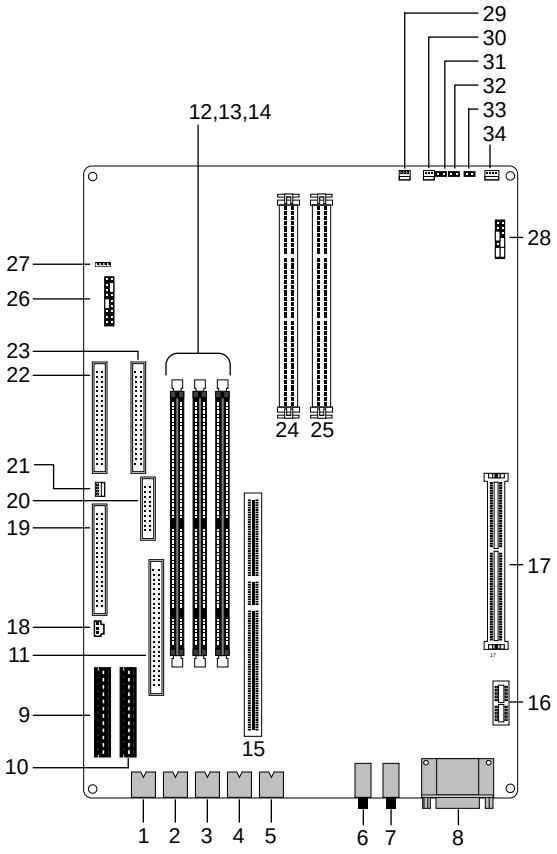


Table 3-1 lists the locations and types of connectors on the Apple Logic Board Design LPX-40. Refer to the connector numbers in Figure 3-1 to determine the location of each connector on the logic board.

Table 3-1 Connectors on the Apple Logic Board Design LPX-40

Location	Description	Connector type
1	PS/2 mouse port	6-pin mini-DIN
2	PS/2 keyboard port	6-pin mini-DIN
3	Apple ADB port	4-pin mini-DIN
4	Apple printer serial port	9-pin mini-DIN
5	Apple modem serial port	9-pin mini-DIN
6	Sound in	Mini-phono jack
7	Sound out	Mini-phono jack
8	Monitor out	15-pin Macintosh or SVGA connector
9	Power supply	12-pin header
10	Power supply	12-pin header
11	SCSI	50-pin header
12	DRAM DIMM slot 3	168-pin connector
13	DRAM DIMM slot 2	168-pin connector
14	DRAM DIMM slot 1	168-pin connector
15	PCI riser connector	192-pin connector
16	GIMO	22-pin connector
17	Video DIMM	120-pin connector
18	Power supply soft power	3-pin header
19	MFM floppy disk drive	34-pin header
20	Apple GCR floppy disk drive	20-pin header
21	CD-audio	4-pin header
22	ATAPI CD-ROM	40-pin header
23	ATA (IDE) hard disk	40-pin header
24	ROM connector	160-pin connector
25	L2 cache connector	160-pin connector
26	Feature options jumper	(6) 3-pin headers
27	Battery connector	4-pin header

continued

Table 3-1 Connectors on the Apple Logic Board Design LPX-40 (continued)

Location	Description	Connector type
28	CPU frequency multiplier (jumper)	(4) 3-pin headers
29	Fan	3-pin header
30	Power LED	3-pin header
31	Reset switch	2-pin header
32	Soft power switch	2-pin header
33	NMI switch	2-pin header
34	Speaker	4-pin header

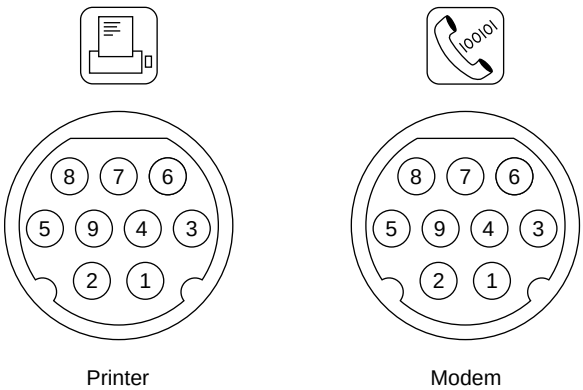
Serial I/O Ports

The Apple Logic Board Design LPX-40 supports four serial ports: two 9-pin mini-DIN serial ports for a printer and a modem and two PS/2 serial ports for a PS/2 keyboard and mouse. The PS/2 ports are strictly for a PS/2 keyboard and mouse and are not general purpose serial I/O channels.

Apple Printer and Modem Ports

The printer and modem serial ports have 9-pin mini-DIN sockets that accept either 8-pin or 9-pin plugs. Both ports support LocalTalk and GeoPort serial protocols. Figure 3-2 shows the mechanical arrangement of the pins on the serial port sockets; Table 3-2 shows the signal assignments.

Figure 3-2 Serial port sockets



Printer Modem

Table 3-2 Serial port signals

Pin	Signal name	Signal description
1	HSKo	Handshake output
2	HSKi	Handshake input (external clock on modem port)
3	TxD–	Transmit data –
4	GND	Ground
5	RxD–	Receive data –
6	TxD+	Transmit data +
7	GPi	General-purpose input (wakeup CPU or perform DMA handshake)
8	RxD+	Receive data +
9	+5 V	+5 volts to external device (100 mA maximum)

Note
Pin 9 on each serial connector provides +5 V power for external devices. The total current available for all devices connected to the +5 V pins on the serial ports, PS/2 ports, and ADB ports is 500 mA. Each external device should draw no more than 100 mA. Excessive current drain will cause a fuse to interrupt the +5 V supply; the fuse automatically resets when the load returns to normal. ◆

Both serial ports include the GPi (general-purpose input) signal on pin 7. The GPi signal for each port connects to the corresponding data carrier detect input on the SCC portion of the O'Hare custom IC, described in Chapter 2. On both serial ports, the GPi line can be connected to the receive/transmit clock (RTxCA) signal on the SCC. That connection supports devices that provide separate transmit and receive data clocks, such as synchronous modems. For more information about the serial ports, see *Guide to the Macintosh Family Hardware,* second edition.

PS/2 Keyboard and Mouse Ports

The Apple Logic Board Design LPX-40 provides two 6-pin mini-DIN PS/2 ports for connection of a PS/2 keyboard and PS/2 mouse. Table 3-3 lists the pin assignments for the PS/2 ports.

Table 3-3 PS/2 port signals

Pin	Signal name	Description
1	Data	Bidirectional data
2	n.c.	Not connected
3	GND	Ground
4	+5 V	+5 V to external device
5	Clock	Bidirectional clock
6	n.c.	Not connected

The PS/2 serial port implementation on the Apple Logic Board Design LPX-40 does not support all permutations of PS/2 keyboards and mouse devices. In particular, only two-button mouse devices that generate a 1 in the sync bit position (bit 3 of the first data byte) of the protocol are supported and only AT-type keyboards are supported. PC keyboards that implement XT or RT key codes are not supported.

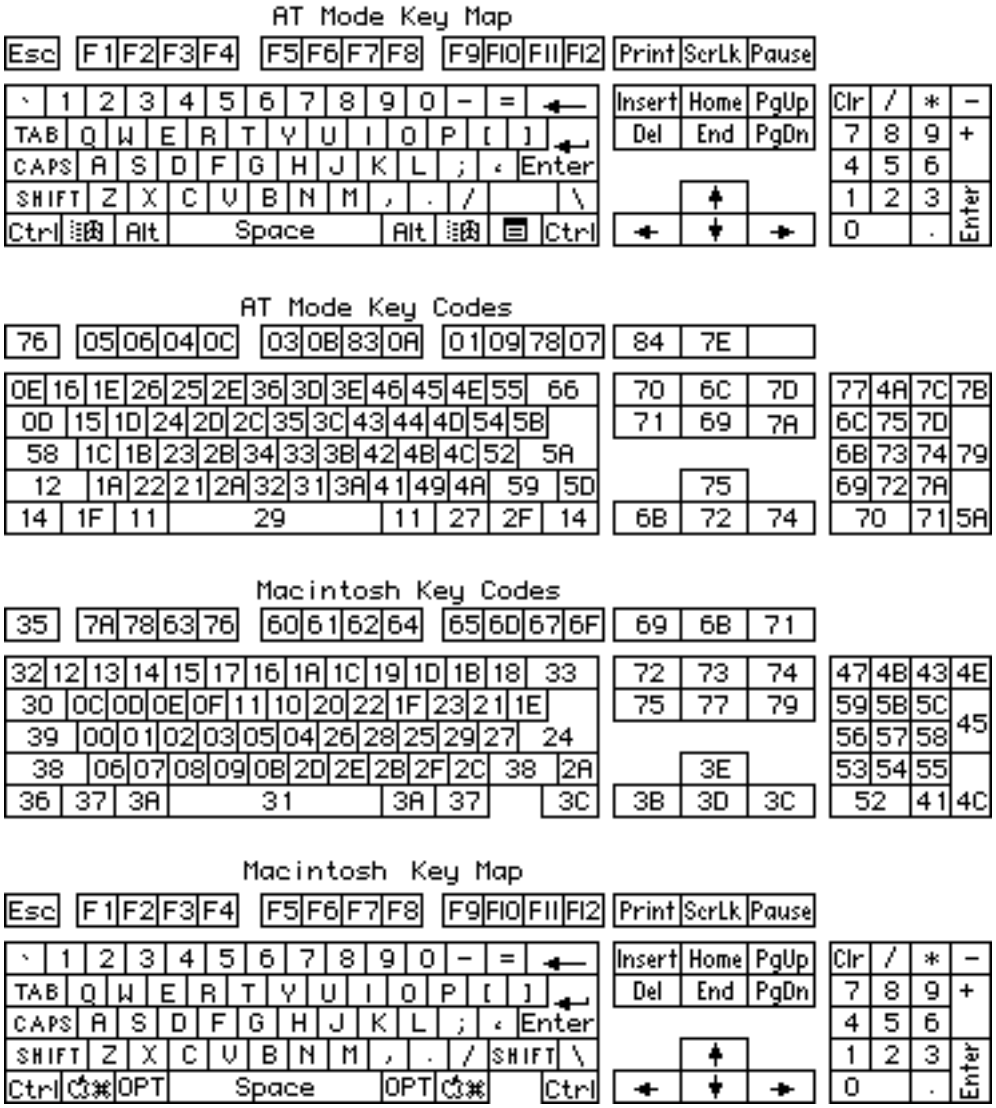
The CudaLite custom IC implements a translation layer that converts the PS/2 device protocols to ADB protocol so that no system ROM or system software changes are required to support PS/2 devices. Because the translation layer is resident within the masked firmware, only a fixed set of PS/2 devices are supported. There is no mechanism for providing translation for alternate PS/2 input devices.

Translation of AT key codes to Macintosh key codes is dependent on the ADB handler ID that is assigned to the keyboard. When the ADB handler ID for the PS/2 keyboard is set to 0x02, translation emulates an ADB extended keyboard with ADB handler ID 0x02, where left and right modifier keys (option, control or shift) return the same Macintosh key codes to the host CPU. When the ADB handler ID for the PS/2 keyboard is set to 0x03, translation emulates an ADB extended keyboard with ADB handler ID 0x03, where left and right modifier keys (option, control, or shift) return unique Macintosh key codes to the host CPU.

The AT keyboard to Macintosh keyboard key maps and key codes for the ID=2 AT key code translation ADB handler are shown in Figure 3-3.

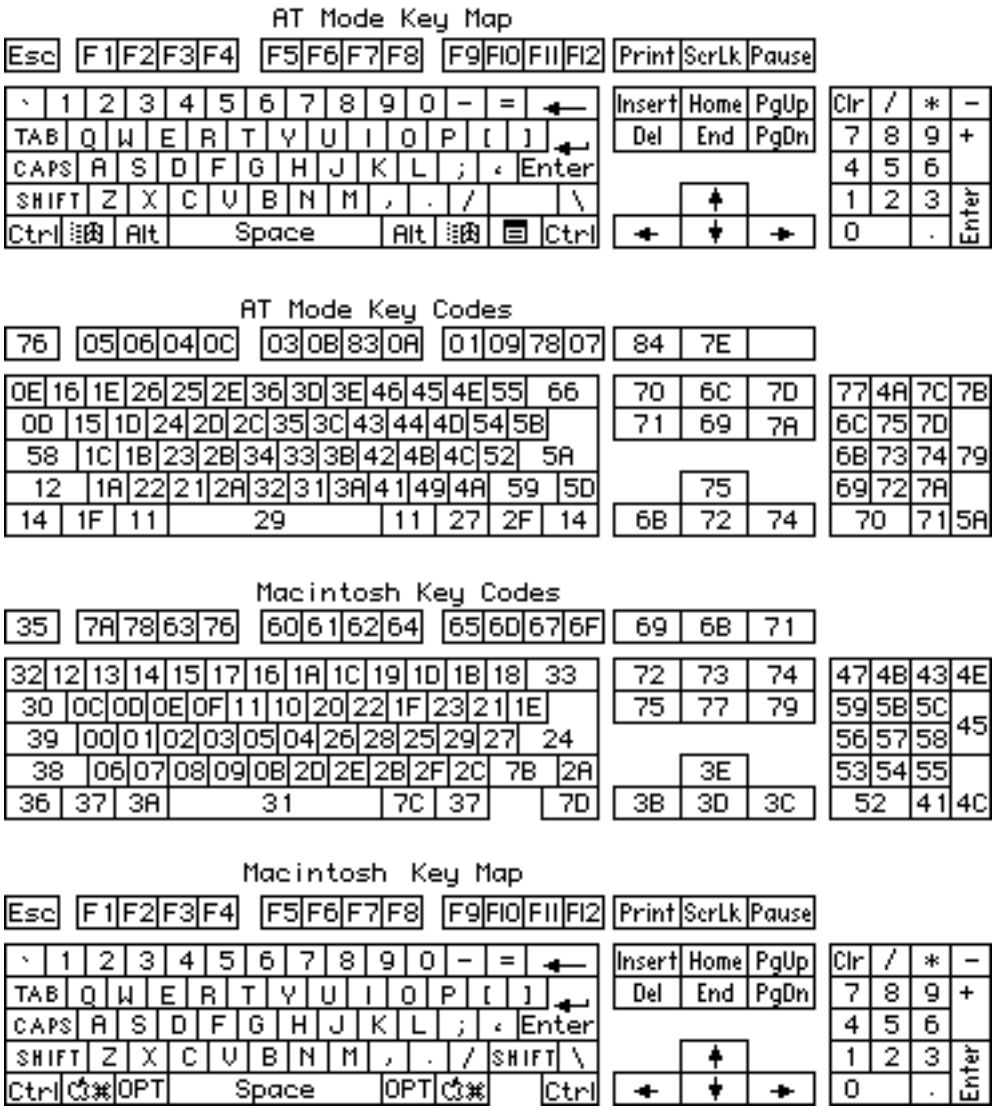
Note
The PS/2 serial ports are strictly for a PS/2 keyboard and mouse. Other devices are not supported on the ports. ◆

Figure 3-3 ADB handler ID=2 key maps and key codes



The AT keyboard to Macintosh keyboard key maps and key codes for the ID=3 AT key code translation ADB handler are shown in Figure 3-4.

Figure 3-4 ADB handler ID=3 key maps and key codes



There is no equivalent ADB key code for the AT keyboard menu key in the Macintosh key codes.

ADB Port

The Apple Desktop Bus (ADB) port on the Apple Logic Board Design LPX-40 is functionally the same as on other Macintosh computers.

The ADB is a single-master, multiple-slave serial communications bus that uses an asynchronous protocol and connects keyboards, graphics tablets, mouse devices, and other devices to the computer. The custom ADB microcontroller drives the bus and reads status from the selected external device. A 4-pin mini-DIN connector connects the ADB to the external devices. Table 3-4 lists the ADB connector pin assignments. For more information about the ADB, see *Guide to the Macintosh Family Hardware*, second edition.

Table 3-4 ADB connector pin assignments

Pin	Signal name	Description
1	ADB	Bidirectional data bus used for input and output. It is an open-collector signal pulled up to +5 volts through a 470-ohm resistor on the main logic board.
2	PSW	Power-on/off signal.
3	+5 V	+5 volts to external device.
4	GND	Ground.

Note
The total current available for all devices connected to the +5 V pins on the ADB, Macintosh serial ports, and PS/2 serial ports is a maximum of 500 mA. Each device should use no more than 100 mA. ◆

Apple ADB Keyboard

The Apple ADB keyboard has a Power key, identified by the symbol ⏻. Pressing the Power key button will turn on the computer. When the user chooses Shut Down from the Special menu, the computer either shuts down or a dialog box appears asking if you really want to shut down. The user can also turn off the power by pressing the Power key.

Enclosures may or may not include a programmer's switch to reset the computer. If an enclosure does not have a programmer's switch, the user invokes the reset and nonmaskable interrupt (NMI) functions by pressing Command key combinations while holding down the Power key, as shown in Table 3-5.

Note
The user must hold down a key combination for at least 1 second to allow the ADB microcontroller enough time to respond to the NMI or hard-reset signal. ◆

Table 3-5 Reset and NMI key combinations

Key combination	Function
Command-Power (⌘-◁)	NMI (always active)
Control-Command-Power (Control-⌘-◁)	Reset

Disk Drives

The Apple Logic Board Design LPX-40 has connectors for one GCR (group code recording) or MFM (modified frequency modulation) internal high-density floppy disk drive, one internal ATA (IDE) hard disk drive, an internal ATAPI CD-ROM drive, and external SCSI devices.

Floppy Disk Drives

The Apple Logic Board Design LPX-40 has connectors for either a GCR or MFM floppy disk drive. The GCR connector is for an internal high-density floppy disk drive (Apple SuperDrive). The MFM connector is for an internal high-density MFM floppy disk drive.

GCR Floppy Disk Drive

The GCR drive is connected with a 20-pin cable that is connected to the main logic board. Table 3-6 shows the pin assignments on the GCR floppy disk connector.

Table 3-6 Pin assignments on the GCR floppy disk connector

Pin	Signal name	Description
1	GND	Ground
2	PH0	Phase 0: state control line
3	GND	Ground
4	PH1	Phase 1: state control line
5	GND	Ground
6	PH2	Phase 2: state control line
7	GND	Ground
8	PH3	Phase 3: register write strobe
9	+5 V	+5 volts
10	/WRREQ	Write data request

continued

Table 3-6 Pin assignments on the GCR floppy disk connector (continued)

Pin	Signal name	Description
11	+5 V	+5 volts
12	SEL	Head select
13	+12 V	+12 volts
14	/ENBL	Drive enable
15	+12 V	+12 volts
16	RD	Read data
17	+12 V	+12 volts
18	WR	Write data
19	+12 V	+12 volts
20	n.c.	Not connected

MFM Floppy Disk Drive

The MFM floppy disk drive is connected with a 34-pin cable that is connected to the main logic board. Table 3-7 shows the pin assignments on the MFM floppy disk connector.

Table 3-7 Pin assignments on the MFM floppy disk connector

Pin	Signal name	Signal description
1	/EJECT	Active-low assertion ejects disk
2	Density_Select	Selects the 700 KB or 1440 KB recording mode
3	Key	Not connected
4	HD_Status	Senses the presence of a 720 KB or 1440 KB disk
5	GND	Ground
6	Disk_In_Place	Senses the presence of a disk in the drive
7	GND	Ground
8	INDEX	Index pulse
9	GND	Ground
10	/FDME0	Motor 0 enable (not used)
11	GND	Ground
12	/FDS1_PD	Drive 1 select (not used)
13	GND	Ground

continued

Table 3-7 Pin assignments on the MFM floppy disk connector (continued)

Pin	Signal name	Signal description
14	/FDS0	Drive 0 select (not used)
15	GND	Ground
16	/FDME1	Motor 1 enable (not used)
17	GND	Ground
18	/DIR	Direction to step
19	GND	Ground
20	/STEP	Step head
21	GND	Ground
22	/WRDATA	Write data
23	GND	Ground
24	/WE	Write enable
25	GND	Ground
26	TRK0	Track zero
27	GND	Ground
28	/WP	Write protect
29	GND	Ground
30	/RDDATA	Read data
31	GND	Ground
32	/HDSEL	Head select
33	GND	Ground
34	/DSKCHG	Disk changed

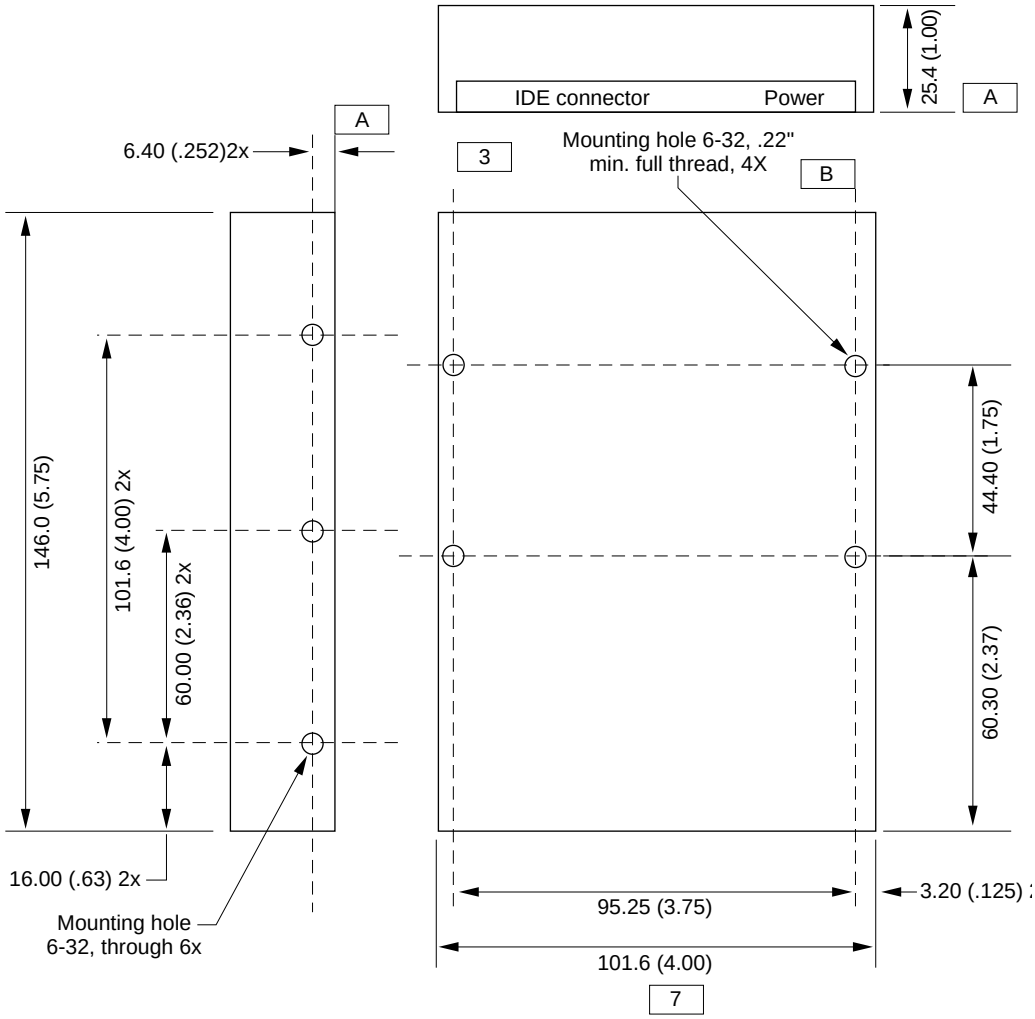
ATA (IDE) Hard Disk

The Apple Logic Board Design LPX-40 has an internal hard disk that complies with the standard ATA-3 interface. This interface, used for ATA drives on IBM AT–compatible computers, is also referred to as the IDE interface. The hard drives used on the Apple Logic Board Design LPX-40 must have software drivers and hardware termination that comply with revision 3.1 of the ATA-3 interface specification.

Hard Disk Specifications

Figure 3-5 shows the maximum dimensions of the hard disk and the location of the mounting holes. As the figure shows, the minimum clearance between conductive components and the bottom of the mounting envelope is 0.5 mm.

Figure 3-5 Maximum dimensions of the hard disk



Notes:

1 A Defined by plane of bottom mount holes

2 B Defined by center line of bottom mount holes

3 40-pin IDE and 4-pin power connector placement must not be reversed

4 Dimensions are in millimeters (inches)

5 Drawing not to scale

6 Tolerances .X = ±0.50, .XX = ±0.25

7 Dimension to be measured at center line of side-mount holes

8 Minimum 0.5 MM clearance from any conductive PCB components to A

Hard Disk Connectors

The internal hard disk has a standard 40-pin ATA connector and a separate 4-pin power connector.

The exact locations of the ATA connector and the power connector are not specified, but the relative positions must be as shown in Figure 3-5 so that the cables and connectors will fit.

Pin Assignments

Table 3-8 shows the pin assignments on the 40-pin ATA (IDE) hard disk connector. A slash (/) at the beginning of a signal name indicates an active-low signal.

Table 3-8 Pin assignments on the ATA (IDE) hard disk connector

Pin number	Signal name	Pin number	Signal name
1	/RESET	2	GROUND
3	DD7	4	DD8
5	DD6	6	DD9
7	DD5	8	DD10
9	DD4	10	DD11
11	DD3	12	DD12
13	DD2	14	DD13
15	DD1	16	DD14
17	DD0	18	DD15
19	GND	20	Key
21	DMA_REQ	22	GROUND
23	DIOW	24	GROUND
25	DIOR	26	GROUND
27	/IORDY	28	Reserved
29	DMA_ACK	30	GROUND
31	INTRQ	32	/IOCS16
33	DA1	34	/PDIAG (not connected)
35	DA0	36	DA2
37	/CS0	38	/CS1
39	/DASP (not connected)	40	GROUND

ATA (IDE) Signal Descriptions

Table 3-9 describes the signals on the ATA (IDE) hard disk connector.

Table 3-9 Signals on the ATA (IDE) hard disk connector

Signal name	Signal description
DA(0–2)	ATA device address; used by the computer to select one of the registers in the ATA drive. For more information, see the descriptions of the CS0 and CS1 signals.
DD(0–15)	DD(0–15) are used to transfer 16-bit data to and from the drive buffer. DD(8–15) are used to transfer data to and from the internal registers of the drive, with DD(0–7) driven high when writing.
DMA_REQ	DMA request.
DMA_ACK	DMA acknowledge.
/CS0	ATA register select signal. It is asserted high to select the additional control and status registers on the ATA drive.
/CS1	ATA register select signal. It is asserted high to select the main task file registers. The task file registers indicate the command, the sector address, and the sector count.
/IORDY	ATA I/O ready; when driven low by the drive, signals the CPU to insert wait states into the I/O read or write cycles.
/IOCS16	ATA I/O channel select; this signal is not used by the O'Hare I/O controller.
DIOR	ATA I/O data read strobe.
DIOW	ATA I/O data write strobe.
INTRQ	ATA interrupt request. This active-high signal is used to inform the computer that a data transfer is requested or that a command has terminated.
/RESET	Hardware reset to the drive; an active-low signal.
Key	This pin is the key for the connector.

CD-ROM Drive

The Apple Logic Board Design LPX-40 has a connector for an internal ATAPI CD-ROM drive. The CD-ROM software supports the worldwide standards and specifications for CD-ROM and CD-digital audio discs described in the Sony/Philips Yellow Book and Red Book. The drive can read CD-ROM, CD-ROM XA, CD-I, and PhotoCD discs as well as play standard audio discs.

The ATA (IDE) hard drive and ATAPI CD-ROM drive are both master devices on the same data bus. Slave ATA (IDE) devices are not supported.

The pin assignments for the ATAPI CD-ROM drive connector are identical to those listed in Table 3-9 for the ATA hard disk drive connector.

SCSI Bus

The Apple Logic Board Design LPX-40 has a SCSI bus for external SCSI devices.

SCSI Connector

The SCSI connector is a 50-pin connector with the standard SCSI pin assignments. The external SCSI connector is a 25-pin D-type connector with the same pin assignments as other Apple SCSI devices. Table 3-10 shows the pin assignments on the internal and external SCSI connectors.

Table 3-10 Pin assignments for the SCSI connectors

Pin number (internal 50-pin)	Pin number (external 25-pin)	Signal name	Signal description
2	8	/DB0	Bit 0 of SCSI data bus
4	21	/DB1	Bit 1 of SCSI data bus
6	22	/DB2	Bit 2 of SCSI data bus
8	10	/DB3	Bit 3 of SCSI data bus
10	23	/DB4	Bit 4 of SCSI data bus
12	11	/DB5	Bit 5 of SCSI data bus
14	12	/DB6	Bit 6 of SCSI data bus
16	13	/DB7	Bit 7 of SCSI data bus
18	20	/DBP	Parity bit of SCSI data bus
25	–	n.c.	Not connected
26	25	TPWR	+5 V terminator power
32	17	/ATN	Attention
36	6	/BSY	Bus busy
38	5	/ACK	Handshake acknowledge
40	4	/RST	Bus reset
42	2	/MSG	Message phase
44	19	/SEL	Select
46	15	/C/D	Control or data

continued

Table 3-10 Pin assignments for the SCSI connectors (continued)

Pin number (internal 50-pin)	Pin number (external 25-pin)	Signal name	Signal description
48	1	/REQ	Handshake request
50	3	/I/O	Input or output
20, 22, 30, 34, and all odd pins except pins 23, 25, and 27	7, 9, 14, 16, 18, and 24	GND	Ground

SCSI Bus Termination

The SCSI bus is terminated internally by a passive terminator. The terminator is located on the main logic board near the SCSI connector.

Sound

The sound system supports both 8-bit and 16-bit stereo sound output and input. The Apple Logic Board Design LPX-40 can create sounds digitally and play the sounds through the internal speaker or send the sound signals out through the sound-output jack. The Apple Logic Board Design LPX-40 also records sound from several sources: a microphone or other sound-input source connected to the sound-input jack or a compact disc in the CD-ROM player. With each sound-input source, sound playthrough can be enabled or disabled.

Sound Output

The Apple Logic Board Design LPX-40 has a connector at the front of the board for built-in speaker support and one sound-output jack at the back of the board. The rear jack is intended for use with external speakers or headphones. The sound-output jack is a stereophonic mini-phono jack. Table 3-11 lists the signal assignments for the sound-output jack.

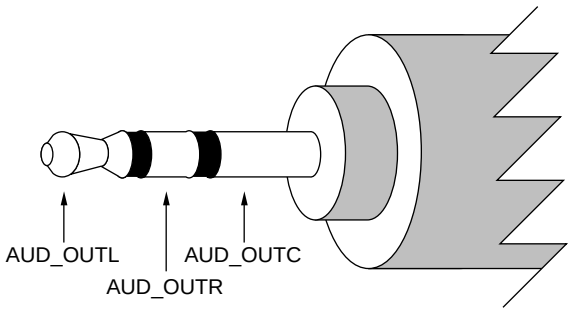
Sound output is controlled by the O'Hare IC. The AWACS IC provides the stereo sound-output to both the internal speaker and the sound-output jacks.

Table 3-11 Signal assignments for the sound output connector

Pin	Signal name	Description
1	AUD_OUTC	Audio-output common
2	AUD_OUTL	Audio-output left channel
3	AUD_OUT_SENSE	Audio-output sense
4	AUD_OUTR	Audio-output right channel
5	n.c.	Not connected
6	Shield	Shield
7	Shield	Shield
8	Shield	Shield

The mini-phono jack for the sound-output port should be wired as shown in Figure 3-6.

Figure 3-6 Mini-phono jack for sound output



Sound Input

The Apple Logic Board Design LPX-40 has a stereo sound-input jack on the back for connecting an external microphone or other sound source. The sound-input jack accepts a standard 3.5-mm stereophonic phone plug (two signals plus ground).

The sound-input jack accepts either the Apple PlainTalk line-level microphone or a pair of line-level signals.

Note
The Apple PlainTalk microphone requires power from the main computer, which it obtains by way of an extra-long, 4-conductor plug that makes contact with a 5-volt pin inside the sound-input jack. ◆

IMPORTANT
The microphone for the Macintosh LC and LC II does not work with the Apple Logic Board Design LPX-40; it requires the line-level signal provided by the Apple PlainTalk microphone. ▲

The available current allowance for the microphone on +5 V is 20 mA.

Sound Input Specifications

The sound input jack has the following electrical characteristics:

- input impedance: 15k ohms
- maximum input level: 1.06 V RMS

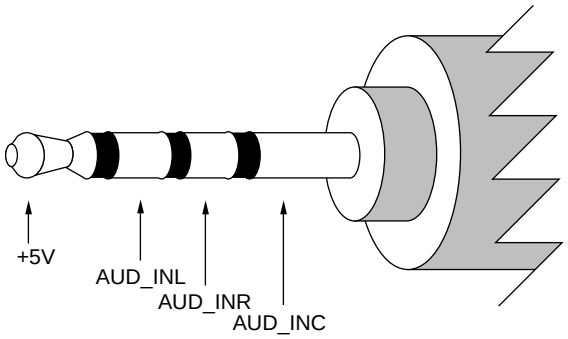
Table 3-12 lists the signal assignments for the sound-input jack.

Table 3-12 Signal assignments for the sound-input jack

Pin	Signal name	Description
1	AUD_INC	Audio-input common
2	AUD_INL	Audio-input left channel
3	AUD_IN_SENSE	Audio-input sense
4	AUD_INR	Audio-input right channel
5	n.c.	Not connected
6	Shield	Shield
7	Shield	Shield
8	Shield	Shield
9	+5 V	Audio microphone +5 V power less than 20 mA
10	MIC_SENSE	Audio microphone sense

Figure 3-7 shows how a PlainTalk compatible mini-phono microphone sound-input jack should be wired.

Figure 3-7 Mini-phono microphone sound-input jack



Digitizing Sound

The Apple Logic Board Design LPX-40 digitizes and records sound as 16-bit samples. The computer can use one of three sampling rates: 11k samples per second, 22k samples per second, and 44k samples per second.

The sound system plays samples at the sampling rate specified in the control panel for sound.

Sound Modes

The sound mode is selected by a call to the Sound Manager. The sound circuitry normally operates in one of three modes:

- Sound playback: computer-generated sound is sent to the speaker and the sound-output jacks.
- Sound playback with playthrough: computer sound and sound input are mixed and sent to the speakers and the sound-output jacks.
- Sound record with playthrough: input sound is recorded and also fed through to the speakers and the sound-output jacks.

When recording from a microphone, applications should reduce the playthrough volume to prevent possible feedback from the speakers to the microphone.

The O'Hare IC provides separate sound buffers for input and for stereo output, so the computer can record and send digitized sound to the sound outputs simultaneously.

Built-in Video

The built-in video circuitry supports pixel display sizes of 512 by 384, 640 by 480, 800 by 600, 832 by 624, 1024 by 768, 1152 by 870, 1280 by 960, and 1280 by 1024. When power is applied, the monitor is initially set for a display size of 640-by-480 pixels. With a multisync monitor the user can switch the monitor resolution on the fly from the

Monitor bit depth and resolution modules in the Control Strip or from the Monitors and Sound control panel.

Video Connectors

The Apple Logic Board Design LPX-40 has an option for either a standard Macintosh 15-pin monitor connector or a standard SVGA high-density 15-pin connector. The pin assignments for the Macintosh 15-pin external monitor connector on the Apple Logic Board Design LPX-40 are shown in Table 3-13.

Table 3-13 Pin assignments for the Macintosh 15-pin external monitor connector

Pin number	Signal name	Description
1	RED Return	Red video ground
2	RED	Red video signal
3	/CSYNC	Composite synchronization signal
4	SENSE0	Apple monitor sense signal 0
5	GREEN	Green video signal
6	GREEN Return	Green video ground
7	SENSE1 (SCL)	Apple monitor sense signal 1 (DDC clock)
9	BLUE	Blue video signal
10	SENSE2 (SDA)	Apple monitor sense signal 2 (DDC data)
11	GND	CSYNC and VSYNC ground
12	/VSYNC	Vertical synchronization signal
13	BLUE Return	Blue video ground
14	GND	HSYNC ground
15	/HSYNC	Horizontal synchronization signal

Figure 3-8 shows the physical pinout for the Macintosh 15-pin external monitor connector.

Figure 3-8 Macintosh 15-pin external monitor connector

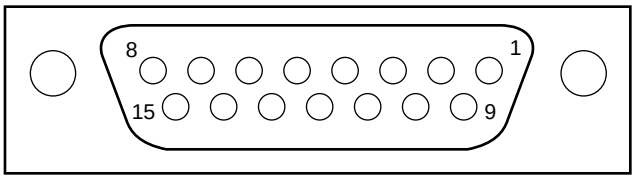


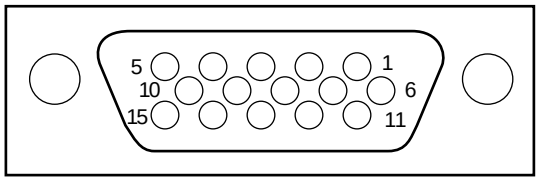
Table 3-14 lists the pin assignments for the optional SVGA 15-pin external monitor connector.

Table 3-14 Pin assignments for the SVGA external monitor connector

Pin	Signal name	Description
1	RED	Red video signal
2	GREEN	Green video signal
3	BLUE	Blue video signal
4	SENSE0	SVGA monitor sense signal 0
5	GND	Ground
6	RED Return	Red video ground
7	GREEN Return	Green video ground
8	BLUE Return	Blue video ground
9	+5 V	+5 V with 0.9A fuse
10	SYNC Return	HSYNC and VSYNC ground
11	SENSE3	SVGA monitor sense signal 3
12	SENSE2 (SDA)	SVGA monitor sense signal 2 (DCC data)
13	/HSYNC	Horizontal or composite synchronization signal
14	/VSYNC	Vertical synchronization signal
15	SENSE1 (SCL)	SVGA monitor sense signal 1 (DCC clock)

Figure 3-9 shows the physical pinout for the SVGA 15-pin external monitor connector.

Figure 3-9 SVGA 15-pin external monitor connector



When the Apple Logic Board Design LPX-40 is configured with the optional SVGA 15-pin monitor connector, an adapter to allow connection to Apple monitors is required. Table 3-15 shows the pin assignments for a SVGA to Macintosh adapter.

Table 3-15 SVGA to Macintosh video adapter pin assignments

SVGA	Description	Macintosh	Description
1	RED	2	RED
2	GREEN	5	GREEN
3	BLUE	9	BLUE
4	SENSE0	4	SENSE0
5	GND	14	HSYNC Return
6	RED Return	1	RED Return
7	GREEN Return	6	GREEN Return
8	BLUE Return	13	BLUE Return
9	+5 V	n.c.	Not connected
10	SYNC Return	14	HSYNC Return
11	SENSE3	12	VSYNC
12	SENSE2 (SDA)	10	SENSE2
13	/HSYNC	15, 3	/HSYNC, /CSYNC
14	/VSYNC	12	/VSYNC
15	SENSE1 (SCL)	7	SENSE1

Video Display Sense Codes

The Apple Logic Board Design LPX-40 supports both Apple and PC compatible monitors. Apple monitors currently use a 15-pin connector that has three signals that are sensed to determine which monitor is connected. The ability to sense the monitor is important, because it makes it possible for the computer to establish a valid video display screen for the user at boot time without any additional user input.

PC compatible monitors use a high density 15-pin SVGA connector that has four pins used for sense signals. The 4-pin sensing scheme has unfortunately been largely ignored and a new video display sensing scheme, referred to as DDC, is used to replace the 4-bit sense code. The DDC (display data channel) sensing scheme uses a serial bit stream from the monitor to determine which resolutions are valid and available.

The sensing sequence differs slightly depending on whether the Apple Logic Board Design LPX-40 is configured with a Macintosh 15-pin or SVGA 15-pin monitor connector.

The monitor sensing sequence for the Macintosh 15-pin configuration is as follows:

1. The DDC sense code is checked. If a valid code is found, sensing is complete.
2. The Apple monitor sense codes are checked. If a valid code is found, sensing is complete.
3. If a load is found on the RGB lines, then a VGA monitor is assumed to be connected and 640-by-480 pixel resolution at 60 Hz is displayed.
4. If no load is found, then video is not displayed.

The monitor sensing sequence for the SVGA 15-pin configuration is as follows:

1. The DDC sense code is checked. If a valid code is found, sensing is complete.
2. If an SVGA to Macintosh video adapter is used, the Apple monitor sense codes are checked. If a valid code is found, sensing is complete.
3. If an SVGA to Macintosh video adapter is used and a load is found on the RGB lines, then a VGA monitor is assumed to be connected and 640-by-480 pixel resolution at 60 Hz is displayed.
4. If no load is found, then video is not displayed.

For every valid sense code, there is a default display mode chosen the first time the computer is started with a monitor attached. The user may change the default display mode to one of the other supported modes, and the system will use the new display mode the next time it is started or returns from a reset with the same monitor attached. If the monitor is switched before the next time the system is started, the default display mode is again chosen. Table 3-16 lists the sense codes, default display modes, valid display modes, and safe display modes for several monitors.

Table 3-16 Video display sense codes

Monitor	Sense code (hex)	Default display mode	Valid display modes	Safe display modes
13-inch color	06 2B	640 x 480	640 x 480	640 x 480
16-inch color	07 2D	832 x 624	832 x 624	832 x 624
19-inch RGB	07 3A	1024 x 768	1024 x 768	1024 x 768
21-inch color two-page	00 XX / 03 XX	1152 x 870	1152 x 870	1152 x 870
Apple MultiScan 14/15-inch	06 03	640 x 480	640 x 480, 800 x 600, 832 x 624, 1024 x 768	640 x 480, 800 x 600, 832 x 624
Apple MultiScan 1705	06 0B	832 x 624	640 x 480, 800 x 600, 832 x 624, 1024 x 768	640 x 480, 800 x 600, 832 x 624, 1024 x 768

continued

Table 3-16 Video display sense codes

Monitor	Sense code (hex)	Default display mode	Valid display modes	Safe display modes
Apple MultiScan 20-inch	06 23	1152 x 870	640 x 480, 640 x 870, 800 x 600, 832 x 624, 1024 x 768, 1152 x 870, 1280 x 960, 1280 x 1024	640 x 480, 640 x 870, 800 x 600, 832 x 624, 1024 x 768, 1152 x 870, 1280 x 960, 1280 x 1024
AppleVision 1710	06 2B	640 x 480	640 x 480, 640 x 870, 800 x 600, 832 x 624, 1024 x 768, 1152 x 870, 1280 x 960, 1280 x 1024	640 x 480, 640 x 870, 800 x 600, 832 x 624, 1024 x 768, 1152 x 870, 1280 x 960, 1280 x 1024
VGA/VESA	07 17	640 x 480	640 x 480, 640 x 870, 800 x 600, 832 x 624, 1024 x 768, 1152 x 870, 1280 x 960, 1280 x 1024	640 x 480

Video Display Resolution

The Apple Logic Board Design LPX-40 supports several resolution sizes for external video monitors. Table 3-17 shows the screen resolutions supported and the maximum pixel depths available for a given amount of video memory. The maximum pixel depth available depends on the monitor's screen resolution setting and the amount of video RAM installed.

Table 3-17 Maximum pixel depths for resolution setting

Screen resolution, in pixels	Vertical refresh, Hz	Horizontal refresh, kHz	Pixel clock, MHz	Maximum pixel depth, in bits per pixel EDO DRAM		Maximum pixel depth, in bits per pixel SGRAM or SDRAM	
				1 MB	2 MB	2 MB	4 MB
512 x 384	70.130	31.488	21.160	16	32	32	32
640 x 480	59.940	31.469	25.175	16	32	32	32
640 x 480	66.667	35.000	30.240	16	32	32	32
640 x 480	72.809	37.861	31.500	16	32	32	32
640 x 480	75.000	37.500	31.500	16	32	32	32
640 x 870	75.000	68.850	57.283	8	16	16	32
800 x 600	60.317	37.879	40.000	16	32	32	32
800 x 600	72.188	48.077	50.000	16	32	32	32
800 x 600	75.000	46.875	49.500	16	32	32	32
832 x 624	74.500	49.725	57.283	8	16	32	32
1024 x 768	60.004	48.363	65.000	8	16	16	32
1024 x 768	70.069	56.476	75.000	8	16	16	16
1024 x 768	75.029	60.023	78.750	8	16	16	16
1152 x 870	75.062	68.681	100.000	8	16	16	16
1280 x 960	75.000	75.000	126.000	na	8	8	16
1280 x 1024	60.020	63.981	108.000	na	8	8	16
1280 x 1024	75.025	79.976	135.000	na	8	8	8

Power Supply

The Apple Logic Board Design LPX-40 can be configured with standard soft or hard-power PS/2 power supplies. A set of jumpers are used to specify which type of

power supply is installed. Power supplies that support energy management features are recommended for conserving energy resources and maintaining low load requirements while the Apple Logic Board Design LPX-40 is in a sleep state.

Power Specifications

Table 3-18 lists the DC power specifications for a 200-watt power supply.

Table 3-18 DC power specifications for a 200-watt power supply

Current type	Maximum current	Maximum power
+5 V	20.0 A	100.0 W
-5.0 V	0.4 A	2.0 W
+5 V (trickle)	0.020 A	0.10 W
+3.3 V	20.0 A	66.0 W
+12 V	7.6 A	92.0 W
-12 V	0.5 A	6.0 W

Note
Total power output cannot exceed 200 W. Total combined power on +5 V and +3.3 V outputs should not be more than 100 W and should not exceed the individual power ratings. ◆

Power Supply Connectors

Table 3-19 lists the pin assignments for the power connectors on the Apple Logic Board Design LPX-40.

Table 3-19 Pin assignments for the power supply connectors

Connector number	Pins	Power values
Power supply connector 1	1	Not connected
	2	+5 V
	3	+12 V
	4*	-12 V (key)
	5	Ground
	6	Ground
Power supply connector 2	1*	Ground (key)
	2	Ground
	3	-5 V
	4	+5 V
	5	+5 V
	6	+5 V
Power supply connector 3	1	3.3 V
	2	3.3 V
	3*	3.3 V (key)
	4	Ground
	5	Ground
	6	Ground
Power supply connector 4	1	3.3 V
	2	3.3 V
	3	3.3 V
	4	Ground
	5*	Ground (key)
	6	Ground
Optional soft-power connector	1*	5 V standby (key)
	2	/PFW power fail warning
	3	Ground
Hard drive power connector	1	+12 V
	2	Ground
	3	Ground
	4	+5V
CD-ROM drive power connector	1	+12 V
	2	Ground
	3	Ground
	4	+5 V
Floppy disk drive power connector	1	+5 V
	2	Ground
	3	Ground
	4	+12 V

CHAPTER 4

Expansion Features

This chapter describes the expansion features supported on the Apple Logic Board Design LPX-40: the DRAM expansion slots, the L2 cache expansion slot, and the PCI expansion slots.

Note
Apple does not support development of third-party second-level (L2) cache cards, because the L2 cache controller is integrated into the design of the cache card. ◆

DRAM DIMMs

The Apple Logic Board Design LPX-40 has three DRAM expansion slots. The DRAM expansion slots accept 3.3 volt EDO unbuffered (extended data output) 8-byte DIMMs (dual inline memory modules). As its name implies, the 8-byte DIMM has a 64-bit-wide data bus.

The DRAM DIMM is an industry standard memory module. Its mechanical design is defined by the JEDEC MO-161-B specification. The electrical design specifications are defined in the JEDEC committee JC-24 specification. The DRAM DIMM connector used on the logic board is Molex part number 71736-0011 or equivalent.

The Apple Logic Board Design LPX-40 supports five banks of memory. DIMM slot 1 supports only single-bank DIMMs. DRAM expansion slots 2 and 3 support both one and two-bank DIMMs. The maximum amount of memory supported on the Apple Logic Board Design LPX-40 is three 32 MB DIMMs, for a total of 96 MB.

The minimum bank size supported by the PSX IC is 4 MB and the largest is 32 MB; the largest DIMM supported is a two-bank DIMM holding 32 MB. Table 4-1 shows the single-bank DRAM DIMM configurations supported in DIMM slot 1 on the Apple Logic Board Design LPX-40.

Table 4-1 DRAM DIMM configurations supported in DIMM slot 1

DIMM size	Device technology	Width	Quantity
8 MB	4 Mbit	1 Mbits x 4	16
8 MB	16 Mbit	1 Mbits x 16	4
16 MB	16 Mbit	2 Mbits x 8	8
32 MB	16 Mbit	4 Mbits x 4	16
32 MB	64 Mbit	4 Mbits x 16	4

IMPORTANT

The number of DRAM devices on a DRAM DIMM is constrained by the load limits of the unbuffered signals. A maximum of two devices can be connected to each data line, a maximum of eight devices can be connected to each /RAS or /CAS line, and a maximum of sixteen devices can be connected to each address line. This limits a DIMM to 32 MB using 16-megabit DRAM devices. ▲

Table 4-2 shows the one and dual-bank DRAM DIMM configurations supported in DIMM slots 2 and 3 on the Apple Logic Board Design LPX-40.

Table 4-2 DRAM DIMM configurations supported in DIMM slots 2 and 3

DIMM size	Device technology	Width	Quantity	Banks
8 MB	4 Mbit	1 Mbits x 4	16	2
8 MB	16 Mbits	1 Mbits x 16	4	1
16 MB	16 Mbits	2 Mbits x 8	8	1
16 MB	16 Mbits	1 Mbits x 16	8	2
32 MB	16 Mbits	4 Mbits x 4	16	1
32 MB	16 Mbits	2 Mbits x 8	16	2
32 MB	64 Mbits	4 Mbits x 16	4	1
64 MB	64 Mbits	4 Mbits x 16	8	2

IMPORTANT

The PSX DRAM controller on the Apple Logic Board Design LPX-40 does not provide support for 4 M by 4 bits with 12 by 10 addressing or 1 M by 16 bits with 12 by 8 or with 11-by-9 addressing DRAM devices. ▲

The only 64-megabit DRAM devices supported on the Apple Logic Board Design LPX-40 must be configured as 4 M by 16 bits with 11-by-11 row and column addressing (not 12 by 10 addressing). Devices configured as 8 M by 8 bits or 16 M by 4 bits will not work, because the maximum memory addressed by a bank is 32 MB.

The DRAM DIMMs can be installed one or more at a time. The Apple Logic Board Design LPX-40 supports only linear memory organization, therefore no performance gains are seen when two DIMMs of the same size are installed. Any size DIMM can be installed in the three DIMM slots, and the combined memory of all of the DIMMs installed will be configured as a contiguous memory space.

DRAM DIMM Connectors

Table 4-3 gives the pin assignments for the 168-pin 3.3 V unbuffered EDO DRAM DIMM connectors.

Table 4-3 Pin assignments on the 3.3 V unbuffered EDO DRAM DIMM connectors

Pin number	Signal name	Pin number	Signal name
1	GND	85	GND
2	D(0)	86	D(32)
3	D(1)	87	D(33)
4	D(2)	88	D(34)
5	D(3)	89	D(35)
6	+3.3 V	90	+3.3 V
7	D(4)	91	D(36)
8	D(5)	92	D(37)
9	D(6)	93	D(38)
10	D(7)	94	D(39)
11	D(8)	95	D(40)
12	GND	96	GND
13	D(9)	97	D(41)
14	D(10)	98	D(42)
15	D(11)	99	D(43)
16	D(12)	100	D(44)
17	D(13)	101	D(45)
18	+3.3 V	102	+3.3 V
19	D(14)	103	D(46)
20	D(15)	104	D(47)
21	Reserved	105	Reserved
22	Reserved	106	Reserved
23	GND	107	GND
24	Reserved	108	Reserved
25	Reserved	109	Reserved
26	+3.3 V	110	+3.3 V
27	/WE(0)	111	Reserved

continued

Table 4-3 Pin assignments on the 3.3 V unbuffered EDO DRAM DIMM connectors (continued)

Pin number	Signal name	Pin number	Signal name
28	/CAS(0)	112	/CAS(4)
29	/CAS(1)	113	/CAS(5)
30	/RAS(0)	114	/RAS(1)
31	/OE(0)	115	Reserved
32	GND	116	GND
33	A(0)	117	A(1)
34	A(2)	118	A(3)
35	A(4)	119	A(5)
36	A(6)	120	A(7)
37	A(8)	121	A(9)
38	A(10)	122	A(11)
39	Not used	123	Not used
40	+3.3 V	124	+3.3 V
41	+3.3 V	125	Reserved
42	Reserved	126	Reserved
43	GND	127	GND
44	/OE(2)	128	Reserved
45	/RAS(2)	129	/RAS(3)
46	/CAS(2)	130	/CAS(6)
47	/CAS(3)	131	/CAS(4)
48	/WE(2)	132	Reserved
49	+3.3 V	133	+3.3 V
50	Not used	134	Not used
51	Not used	135	Not used
52	Not used	136	Not used
53	Not used	137	Not used
54	GND	138	GND
55	D(16)	139	D(48)
56	D(17)	140	D(49)
57	D(18)	141	D(50)
58	D(19)	142	D(51)

continued

Table 4-3 Pin assignments on the 3.3 V unbuffered EDO DRAM DIMM connectors (continued)

Pin number	Signal name	Pin number	Signal name
59	+3.3 V	143	+3.3 V
60	D(20)	144	D(52)
61	Not used	145	Not used
62	Not used	146	Not used
63	Not used	147	Not used
64	GND	148	GND
65	D(21)	149	D(53)
66	D(22)	150	D(54)
67	D(23)	151	D(55)
68	GND	152	GND
69	D(24)	153	D(56)
70	D(25)	154	D(57)
71	D(26)	155	D(58)
72	D(27)	156	D(59)
73	+3.3 V	157	+3.3 V
74	D(28)	158	D(60)
75	D(29)	159	D(61)
76	D(30)	160	D(62)
77	D(31)	161	D(63)
78	GND	162	GND
79	Not used	163	Not used
80	Not used	164	Not used
81	Not used	165	Not used
82	Not used	166	Not used
83	Not used	167	Not used
84	+3.3 V	168	+3.3 V

Table 4-4 describes the signals on the RAM DIMM connector.

Table 4-4 RAM DIMM signals

Signal name	Description
A(11:0)	Address inputs
/CAS(7:0)	Column address strobe signals
D(63:0)	Data input and output signals
/OE(0, 2)	Output enable signals
/RAS(3:0)	Row address strobe signals; /RAS(0) and /RAS(2) are Bank 1; /RAS(1) and /RAS(3) are Bank 2
Reserved	Reserved, don't use
+3.3V	+3.3 V power
GND	Ground
/WE(0, 2)	Read/write input signals

RAM Address Multiplexing

Signals A[11:0] on each RAM DIMM make up a 12-bit multiplexed address bus that can support several different types of DRAM devices. Table 4-5 shows the address multiplexing modes used with several types of DRAM devices. The devices are characterized by their bit dimensions: for example, a 4 M by 4-bit device has 4-M addresses and stores 4 bits at a time.

Table 4-5 Address multiplexing modes for various DRAM devices

Device size	Device type	Size of row address	Size of column address
4 Mbits	1 M by 4 bits	10	10
16 Mbits	1 M by 16 bits	10	10
16 Mbits	2 M by 8 bits	11	10
16 Mbits	2 M by 8 bits	12	9
16 Mbits	4 M by 4 bits	11	11

Table 4-6 shows how the address signals to the RAM devices are multiplexed during the row and column address phases for noninterleaved banks.

Table 4-6 Address multiplexing in noninterleaved banks

	Individual signals on the DRAM_ADDR bus											
	A(11)	**A(10)**	**A(9)**	**A(8)**	**A(7)**	**A(6)**	**A(5)**	**A(4)**	**A(3)**	**A(2)**	**A(1)**	**A(0)**
Row address	22	23	21	20	19	18	17	16	15	14	13	12
Column address		24	22	11	10	9	8	7	6	5	4	3

RAM Devices

The memory controller in the PSX IC supports 4 Mbit and 16 Mbit 3.3 V unbuffered EDO DRAM devices. The access time (T_{RAS}) of the DRAM devices is 60 ns or faster.

RAM Refresh

The PSX IC provides a CAS-before-RAS refresh cycle every 15.6 µs. DRAM devices must be compatible with this refresh cycle; for example, this cycle will refresh 2K-refresh parts within 32 milliseconds.

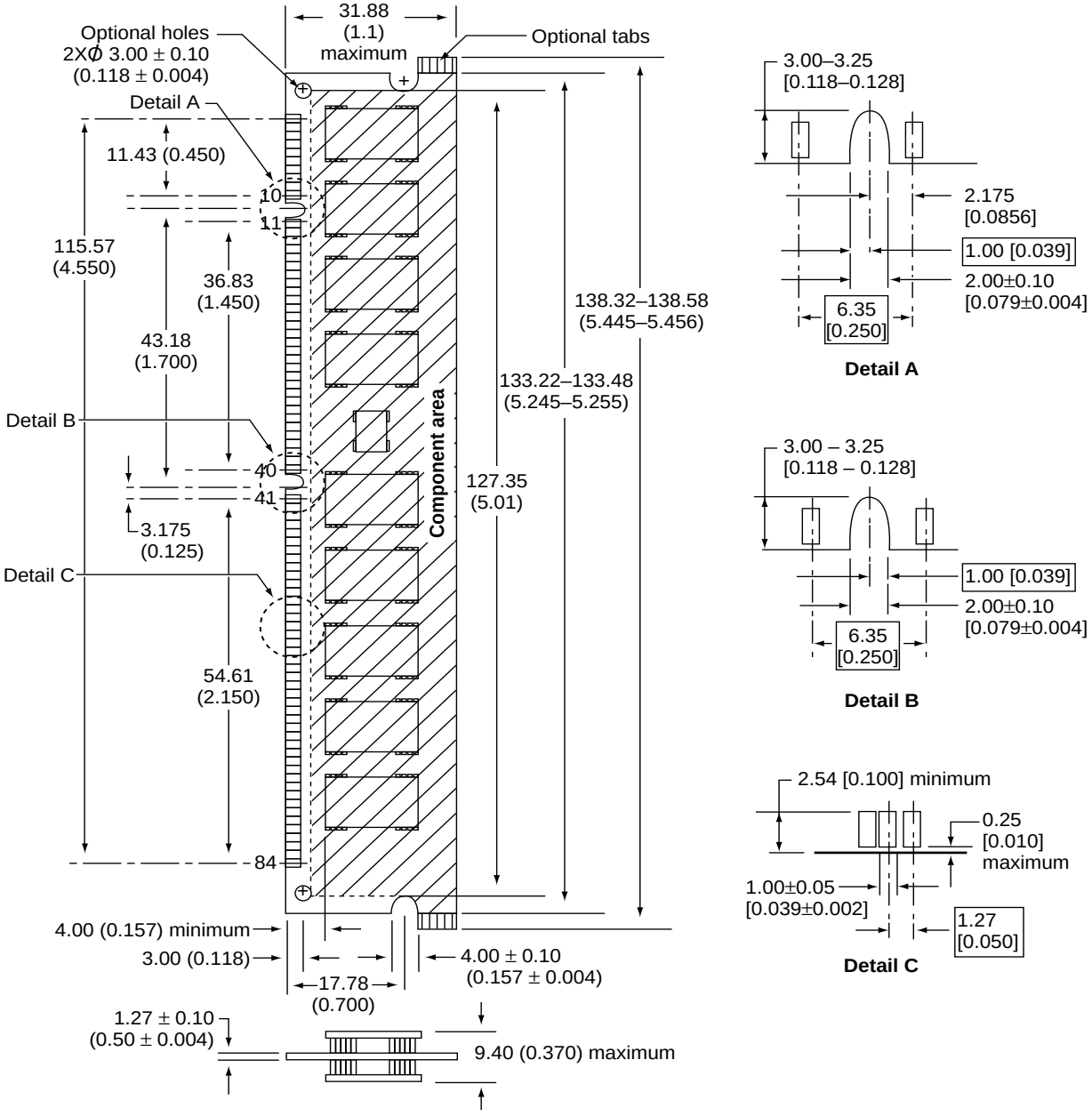
RAM DIMM Dimensions

Figure 4-1 shows the dimensions of the RAM DIMM.

IMPORTANT

The JEDEC MO-161-B specification shows three possible heights for the DRAM DIMM. For Macintosh computers, developers should use only the shortest of the three: 1.100 inches. Taller DIMMs put excessive pressure on the DIMM sockets due to possible mechanical interference inside the case. ▲

Figure 4-1 Dimensions of the RAM DIMM



Note: dimensions are in millimeters (inches)

Second-Level Cache DIMM

The Apple Logic Board Design LPX-40 has a slot for a second-level (L2) cache on a DIMM.

The L2 cache DIMM contains the cache controller, tag, and data store memory. It is a lookaside cache, which is connected to the PowerPC processor bus.

Table 4-7 shows the pin and signal assignments on the L2 cache DIMM connector.

Table 4-7 Pin and signal assignments for the L2 cache DIMM connector

Pin	Signal name	Pin	Signal name	Pin	Signal name	Pin	Signal name
1	+5 V	41	A15	81	D63 (LSB)	121	A16
2	D31	42	A13	82	D62	122	A14
3	D30	43	+3.3 V	83	D61	123	A12
4	D29	44	A11	84	GND	124	A10
5	D28	45	A9	85	D60	125	A8
6	D27	46	A7	86	D59	126	GND
7	+5 V	47	A5	87	D58	127	A6
8	D26	48	A3	88	D57	128	A4
9	D25	49	+3.3 V	89	D56	129	A2
10	D24	50	A1	90	GND	130	A0 (MSB)
11	D23	51	/WT	91	D55	131	/DBB
12	D22	52	/GBL	92	D54	132	GND
13	+5 V	53	Reserved	93	D53	133	/CPU_BG
14	D21	54	/SRESET	94	D52	134	/CPU_BR
15	D20	55	+3.3 V	95	D51	135	L2_PRSNT
16	D19	56	TTYPE0	96	GND	136	Reserved
17	D18	57	TTYPE1	97	D50	137	TSIZ0
18	D17	58	TTYPE2	98	D49	138	GND
19	+5 V	59	TTYPE3	99	D48	139	TSIZ1
20	D16	60	TTYPE4	100	/CACHE_EN	140	TSIZ2
21	/L2_BR	61	+3.3 V	101	/TBST	141	/SHD
22	/L2_BG	62	D15	102	GND	142	D47

continued

Table 4-7 Pin and signal assignments for the L2 cache DIMM connector (continued)

Pin	Signal name	Pin	Signal name	Pin	Signal name	Pin	Signal name
23	TC0	63	D14	103	/CI	143	D46
24	TC1	64	D13	104	/RSRV	144	GND
25	+3.3 V	65	D12	105	Reserved	145	D45
26	/HRESET	66	D11	106	/CACHE_HIT	146	D44
27	/TEA	67	+5 V	107	/AACK	147	D43
28	/TS	68	D10	108	GND	148	D42
29	GND	69	D9	109	/TA	149	D41
30	SYS_CLK	70	D8	110	/ARTRY	150	GND
31	+3.3 V	71	D7	111	/ABB	151	D40
32	A31 (LSB)	72	D6	112	A30	152	D39
33	A29	73	+5 V	113	A28	153	D38
34	A27	74	D5	114	GND	154	D37
35	A25	75	D4	115	A26	155	D36
36	A23	76	D3	116	A24	156	GND
37	+3.3 V	77	D2	117	A22	157	D35
38	A21	78	D1	118	A20	158	D34
39	A19	79	+5 V	119	A18	159	D33
40	A17	80	D0 (MSB)	120	GND	160	D32

Table 4-8 defines the signals on the L2 cache DIMM connector.

Table 4-8 Signal descriptions for L2 cache DIMM connector

Signal name	Description
+5 V	Power supply voltage of +5 volts for tag RAM (5% tolerance)
+ 3.3 V	Power supply voltage of +3.3 volts for data RAM (5% tolerance)
GND	Ground
A(0-31)	Processor address bus signals 0 through 31
D(0-63)	Processor data bus signals 0 through 63; sampled on the rising edge of the CLK signal during a write cycle
/AACK	Address acknowledge, same as AACK_ signal on PowerPC 603e
/ARTRY	Address retry, same as ARTRY_ signal on PowerPC 603e

continued

Table 4-8 Signal descriptions for L2 cache DIMM connector (continued)

Signal name	Description
/ABB	Address bus busy, same as ABB_ signal on PowerPC 603e
/CI	Cache inhibit, same as CI_ signal on PowerPC 603e
/CPU_BG	Bus transaction granted, same as BG_ signal on PowerPC 603e
/CPU_BR	Bus transaction requested, same as BR_ signal on PowerPC 603e
/DBB	Data bus busy, same as DBB_ signal on PowerPC 603e
/GBL	Global transaction
/HRESET	Main logic board hardware reset
/L2_BG	Bus grant to L2 cache; used only in copyback mode
/L2_BR	Bus request from L2 cache; used only in copyback mode
CACHE_EN	Enables cache when high
L2_PRSNT	L2 cache present; tied directly to power rail on cache DIMM
/CACHE_HIT	Indicates L2 cache will source the data for the current cycle; inhibits main logic board memory controller
/RSRV	Reservation signal, same as RSRV_ signal on PowerPC 603e
Reserved	Do not use
/SHD	Shared, not used
/SRESET	Soft reset, same as SRESET_ signal on PowerPC 603e
SYS_CLK	System clock, same as SYSCLOCK signal on PowerPC 603e
/TA	Transfer acknowledge, same as TA_ signal on PowerPC 603e
/TBST	Transfer burst in progress, same as TBST_ signal on PowerPC 603e
TC(0-1)	Transfer code, same as TC signal on PowerPC 603e
/TEA	Transfer error acknowledge, same as TEA_ signal on PowerPC 603e
/TS	Transfer start signal, same as TS_ signal on PowerPC 603e
TSIZ (0-2)	Transfer size for the data transaction
TTYPE(0-4)	Transfer type, same as TT signal on PowerPC 603e
/WT	Write-through, same as WT_ signal on PowerPC 603e

Video RAM

The Apple Logic Board Design LPX-40 has a 120-pin video DIMM connector that allows the use of +5 V EDO DRAM, +3.3 V SDRAM, and +3.3 V SGRAM for video RAM

expansion. The video DIMM connector used on the Apple Logic Board Design LPX-40 is Burndy Corporation's part number ELF120GSC-3Z50 or equivalent. The connector is designed to support the pinout of the ATI 264VT-A4S2 graphics controller. The graphics controller recognizes the presence of pullup resistors on certain data bits on the DIMM to determine which type of memory is present. The video controller supports 1, 2, or 4 MB of RAM for video memory.

Note
No video performance advantage is gained with EDO video DIMMs larger than 2 MB. A 4-MB SGRAM or SDRAM video DIMM provides higher bandwidth performance resulting in greater pixel depth. ◆

Table 4-9 shows the pin and signal assignments on the video DIMM connector.

Table 4-9 Pin and signal assignments on the 120-pin video DIMM connector

Pin	Signal name	Pin	Signal name
1	GND	61	GND
2	VA0	62	VA1
3	VA2	63	VA3
4	VA4	64	VA5
5	VA6	65	VA7
6	+5 V	66	+5 V
7	VA8	67	VA9
8	Reserved	68	Reserved
9	/VOE(0) (CLK)	69	/VOE(1) (/WE)
10	/VWE(0) (/CAS0)	70	/VWE(1) (/CAS1)
11	GND	71	GND
12	/VRAS(0)	72	/VRAS(1)
13	/VCAS(0)	73	/VCAS(1)
14	/VCAS(2)	74	/VCAS(3)
15	/VCAS(4)	75	/VCAS(5)
16	+3.3 V	76	+3.3 V
17	/VCAS(6)	77	/VCAS(7)
18	VMD0	78	VMD1
19	VMD2	79	VMD3
20	VMD4	80	VMD5

continued

Table 4-9 Pin and signal assignments on the 120-pin video DIMM connector (continued)

Pin	Signal name	Pin	Signal name
21	GND	81	GND
22	VMD6	82	VMD7
23	VMD8	83	VMD9
24	VMD10	84	VMD11
25	VMD12	85	VMD13
26	+5 V	86	+5 V
27	VMD14	87	VMD15
28	VMD16	88	VMD17
29	VMD18	89	VMD19
30	VMD20	90	VMD21
31	GND	91	GND
32	VMD22	92	VMD23
33	VMD24	93	VMD25
34	VMD26	94	VMD27
35	VMD28	95	VMD29
36	+3.3 V	96	+3.3 V
37	VMD30	97	VMD31
38	VMD32	98	VMD33
39	VMD34	99	VMD35
40	VMD36	100	VMD37
41	GND	101	GND
42	VMD38	102	VMD39
43	VMD40	103	VMD41
44	VMD42	104	VMD43
45	VMD44	105	VMD45
46	+5 V	106	+5 V
47	VMD46	107	VMD47
48	VMD48	108	VMD49
49	VMD50	109	VMD51
50	VMD52	110	VMD53

continued

Table 4-9 Pin and signal assignments on the 120-pin video DIMM connector (continued)

Pin	Signal name	Pin	Signal name
51	GND	111	GND
52	VMD54	112	VMD56
53	VMD56	113	VMD57
54	VMD58	114	VMD59
55	VMD60	115	VMD61
56	+3.3 V	116	+3.3 V
57	VMD62	117	VMD63
58	DSF	118	/CS0
59	Reserved	119	/CS1
60	Reserved (STERM_PWR)	120	Reserved (STERM_GND)

The signal names enclosed in parenthesis are used for SDRAM and SGRAM DIMMs. The signals (STERM_PWR) on pin 60 and (STERM_GND) on pin 120 are connected to +3.3 V and GND respectively. The (STERM_PWR) and (STERM_GND) pins must not be connected on EDO DRAM DIMMs.

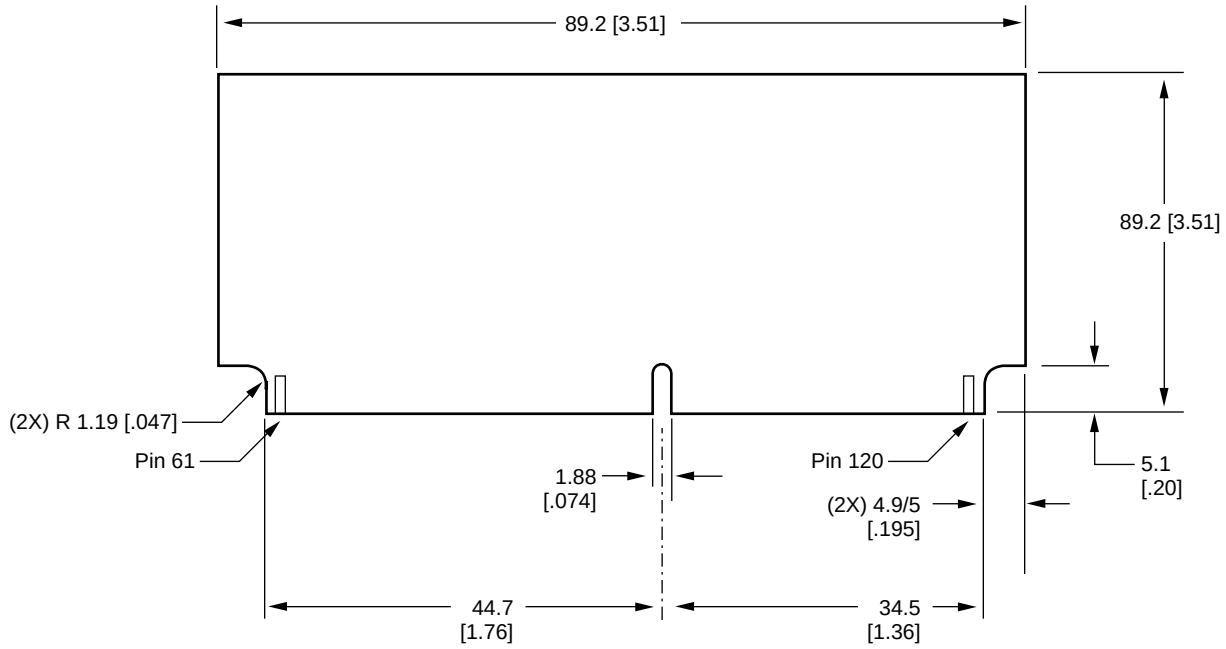
Video RAM DIMM Card

Video RAM DIMM cards for the Apple Logic Board Design LPX-40 must be constructed as a four or more layer PCB substrate with one of the conductive layers on the PCB used for ground, not for signal routing. The dimensions for a 120-pin video DIMM card are shown in Figure 4-2.

EDO DRAM devices should be dual CAS with 60 ns access time or faster. A 1 MB EDO video DRAM DIMM card comprises two 256K by 16-bit EDO DRAM devices and a 2 MB EDO video DRAM DIMM card comprises four 256K by 16-bit EDO DRAM devices. EDO video DRAM DIMM cards requires 10K pullup resistors connected to data lines VMD48, VMD50, and VMD51.

A 2 MB SGRAM video DIMM card comprises two 256K by 32-bit SGRAM devices and a 4 MB SGRAM video DIMM card comprises four 256K by 32-bit SGRAM devices. The ATI264VT-A4S2 graphics controller on the Apple Logic Board Design LPX-40 clocks the SGRAM and SDRAM at 66 MHz. SGRAM and SDRAM video DIMM cards require 10K pullup resistors connected to data lines VMD48 and VMD49. The clock (CLK) signal termination resistors for SDRAM and SGRAM video DIMM cards should be placed close to the end of the clock trace on the DIMM card.

Figure 4-2 Video DIMM card dimensions



You can request additional information about the electrical design specifications for video DRAM DIMM cards that are compatible with the LPX-40 logic board, by sending an email request to DevSupport@Apple.com

PCI Expansion Slot

The Apple Logic Board Design LPX-40 uses the industry-standard peripheral component interconnect (PCI) bus for an I/O expansion bus. The PCI bus is a 32-bit multiplexed address and data bus. The PCI expansion slot has a 33.33 MHz system clock.

PCI I/O expansion cards are mounted horizontally in a 90-degree straight-through adapter board, which is installed in the PCI expansion slot on the main logic board.

IMPORTANT

The Apple Logic Board Design LPX-40 requires that PCI cards use the 5-volt signaling standard described in the *PCI Local Bus Specification*, Revision 2.0. ▲

The Apple Logic Board Design LPX-40 accepts standard 6.88-inch PCI cards as defined by the *PCI Local Bus Specification*, Revision 2.0. The cards are required to use the standard ISA fence described in the specification.

The PCI slots support all the required PCI signals and certain optional PCI signals. The supported PCI signals are listed in Table 4-4.

Table 4-10 PCI signals

Signal name	Description
AD [0–31]	Address and data, multiplexed
C/BE[0–3]	Bus command and byte-enable signals, multiplexed
PAR	Parity; used with AD and C/BE signals
FRAME#	Cycle frame; asserted to indicate a bus transaction
TRDY#	Target ready; selected device is able to complete the current phase
IRDY#	Initiator ready; master device is able to complete the current phase
STOP#	Stop; indicates the current target device is requesting the master to stop the current transaction
DEVSEL#	Device select; indicates that the driving device has decoded its address as the target of the current access
IDSEL	Initialization device select; used during configuration
REQ#	Request; indicates to the arbiter that the asserting agent requires access to the bus
GNT#	Grant; indicates to the agent that access to the bus has been granted
CLK	Clock; rising edge provides timing for all transactions
RST#	Reset; used to bring registers and signals to a known state
INTA#, INTB#, INTC#, INTD#	Interrupt request pins; wired together on each slot
LOCK#	Lock; indicates an operation that may require multiple transactions to complete
PERR#	Parity error; used to report data parity errors during PCI transactions excluding a Special Cycle transaction
SERR#	System error; used to report address parity errors, data parity errors during a Special Cycle, or any other system error that will be catastrophic

The PCI slots on the Apple Logic Board Design LPX-40 do not support the optional 64-bit bus extension signals or cache support signals.

For more information about the PCI expansion slot, refer to *Designing PCI Cards and Drivers for Power Macintosh Computers.*

CHAPTER 5

MFM Floppy Disk Device Driver

The Apple Logic Board Design LPX-40 includes I/O for GCR (group code recording) and MFM (modified frequency modulation) floppy disk drives. The purpose behind the addition of MFM support is to give customers an inexpensive floppy drive solution on a Macintosh compatible platform. The MFM floppy disk driver is the Mac OS software that controls the drive.

About the MFM Floppy Disk Driver

The full-featured floppy disk drives and associated floppy drive controller hardware, used on all of the Apple Macintosh desktop computer line built before the LPX-40 logic board are GCR compatible floppy drives. For developers interested in building Macintosh compatible computers, the MFM floppy drive provides an inexpensive alternative to the expensive and not readily available GCR compatible floppy drive. The MFM floppy drive solution also gives users of future Macintosh computers a low-cost, readily available, PC industry standard floppy drive replacement option.

Older models of Macintosh computers that use GCR floppy drives support 400K, 800K, and 1.44 MB capacity formats, as well as software-controlled media eject, and in the distant past, auto insert. The MFM floppy drive implementation on the initial release of the LPX-40 logic board design supports manual eject and manual insert, but does not support 400K and 800K GCR encoding formats.

Auto eject is fully supported by the MFM driver when the appropriate jumpers on the LPX-40 logic board are set and an auto-eject MFM floppy drive is installed.

IMPORTANT

Data loss can occur when a 400K or 800K floppy disk with known good data is inserted in the MFM floppy drive, because the driver reports that the disk is blank and allows the user to format the disk. ▲

The MFM floppy disk driver is designed to work with a floppy disk drive controller that implements the industry-standard system software interface and hardware pinout to the drive. On the LPX-40 logic board the floppy disk controller is connected to and works in conjunction with the O'Hare DMA controller ASIC to control the I/O operations of the floppy drive.

The MFM drive is an industry standard 3.5 inch MFM-only floppy disk drive with the following required features:

- a Disk In Place output signal on pin 6 (this output signal must be functional when the drive motor is on or off)
- a Media Density Sense output signal on pin 4 (this output signal is not required to be functional when the drive motor is off, but it must work when the drive motor is on)

The hardware requirements allow the driver to detect the disk presence status and the disk capacity, which reduces the impact of the considerable feature differences between the GCR and MFM floppy drive implementation on the Macintosh.

Using the MFM Floppy Disk Driver

The MFM floppy disk driver is a Mac OS driver of type `DRVR` as described in *Inside Macintosh: Devices* and *Designing Cards and Drivers for the Macintosh Family*, third edition. The MFM floppy disk driver is a ROM based driver, which is initialized by the system at boot time.

The name of the driver in the driver file header is `.Sony` for compatibility with programs that walk the unit table looking for that string.

MFM Floppy Driver API Reference

This section describes the parameter block interface to the synchronous and asynchronous variations of the read and write calls and all of the variations of Control and Status calls implemented for the MFM floppy driver application programming interface (API). The main client of the driver is the file system. However, applications may from time to time also make direct calls to this driver.

You must understand how the Mac OS Device Manager works and be familiar with how to call device drivers on Macintosh computers to use the information included in this section. See *Inside Macintosh: Devices* for more information about device drivers.

Read and Write Prime Routines

A general description of the read and write calls to Macintosh device drivers is provided in the Device Manager chapter of Inside Macintosh, Volume II. This section supplements that information.

The Device Manager prime routines expect the following fields in the I/O parameter block to be set up:

`ioCompletion`	Contains a pointer to a completion routine for asynchronous calls, or nil for synchronous calls
`ioVRefNum`	The drive number for device calls or the volume reference number for file system calls
`ioRefNum`	Driver reference number (guaranteed to be -5 for floppy disks)
`ioBuffer`	A pointer to the location in memory where data is read to or written from
`ioReqCount`	Number of bytes to read from or write to the disk
`ioPosMode`	Contains the absolute starting point: beginning, end, or current location (bit 6 will be set to 1 to do a read-verify instead of a read)
`ioPosOffset`	Offset in bytes relative to the starting point specified in `ioPosMode`

When the driver prime routine is called, register A0 points to the I/O parameter block, and register A1 points to the Device Control Entry (DCE) for the driver. The device manager sets the `ioTrap` field of the parameter block to either 0xA002 for a read request or 0xA003 for a write request so that the driver can determine what action to take. Also, the `dCtlPosition` field in the driver DCE is set to the starting byte offset relative to the beginning of the disk.

The driver can only be called synchronously or asynchronously. Making an immediate mode call to the driver causes it to fail. The driver begins a read or write request and returns control immediately to the caller, which is either the user (asynchronous) or the Device Manager (synchronous), then completes the request asynchronously at the interrupt level. When the request is completed or terminated, the driver returns one of the result codes listed in Table 5-1.

Table 5-1 Read and write prime routine result codes

Name	Number	Description
`noErr`	0	Successful, no error occurred
`wPrErr`	-44	Diskette is write protected
`paramErr`	-50	Some of the requested blocks are past the end of the disk, or `ioReqCount` is not an even multiple of 512 bytes
`nsDrvErr`	-56	No such drive number
`noDriveErr`	-64	Drive not present
`offLinErr`	-65	Read or write request made to an ejected disk
`noNybErr`	-66	Couldn’t find 5 nibbles in 200 tries (GCR) or byte timeout (MFM)
`noAdrMkErr`	-67	Couldn’t find a valid address mark
`dataVerErr`	-68	Read verify compare failed
`badCkSmErr`	-69	Address mark checksum was incorrect
`badBtSlpErr`	-70	One of the address mark bit slip nibbles was incorrect (GCR)
`noDtaMkErr`	-71	Couldn’t find a data mark header
`badDCkSum`	-72	Bad data mark checksum
`badDBtSlp`	-73	One of the data mark bit slip nibbles was incorrect (GCR)
`wrUnderRun`	-74	Couldn't write fast enough to keep up with the IWM
`cantStepErr`	-75	Step handshake failed during seek
`tk0BadErr`	-76	Track 0 detect sensor doesn’t change during a head recalibration

continued

Table 5-1 Read and write prime routine result codes (continued)

Name	Number	Description
`initIWMErr`	-77	Unable to initialize IWM floppy controller
`twoSideErr`	-78	Tried to read a double-sided disk on a single-sided drive
`spdAdjEr`	-79	Unable to correctly adjust the drive speed (GCR, 400K drives only)
`seekErr`	-80	Wrong track number read in a sector's address field
`sectNFErr`	-81	Sector number never found on a track

Control Calls

Control calls perform all of the non-read/write operations on a particular disk associated with this driver. The control opcode is passed to the driver in the `csCode` field of the I/O parameter block (byte 26). Control calls that return information pass it back starting at the `csParam` field of the I/O parameter block (byte 28). A description of each control operation is given below along with any result codes it returns.

Kill I/O

The Kill I/O control call terminates any current I/O request in progress.

The Kill I/O control call has a `csCode` of 1.

The MFM driver does not support this control call and always returns a result code of -1.

Verify Disk

The Verify Disk control call reads every sector from the selected disk to verify that all sectors have been written correctly. If any sector is found to be bad, it terminates immediately and returns an error code.

The Verify Disk control call has a `csCode` of 5.

The possible result codes returned by this control call are:

`noErr`	0	No error
`controlErr`	-17	Verify failed
`nsDrvErr`	-56	No such drive number
`noDriveErr`	-64	Drive not installed
`noNybErr`	-66	Various read errors
`badDBtSlp`	-73	One of the data mark bit slip nibbles was incorrect (GCR)
`cantStepErr`	-75	Step handshake failed during seek

`initIWMErr`	-77	Unable to initialize IWM
`spdAdjErr`	-79	Unable to correctly adjust disk speed (GCR)
`verErr`	-84	Track failed to verify

Format Disk

The Format Disk control call writes address headers and data fields for every sector on the disk and (for GCR disks only) does a limited verification of the format by checking that the address field of the first sector on each track can be read. If any error occurs (including write-protected media), the formatting is aborted and an error code is returned.

The Format Disk control call has a `csCode` of 6.

The `csParam` field is used to specify the type of formatting to be done on floppy disks only. In pre-SWIM (SWIM1 through SWIM3 are Macintosh GCR floppy disk controllers) versions of the driver, putting a 0x0001 at `csParam` creates a single-sided disk, and a non-0x0001 (usually 0x0002) creates a double-sided disk. In the SWIM and later versions, this value is an index into a list of possible formats for the given hardware/disk combination, as returned by the Return Format List status call described on page 5-77.

The possible result codes returned by this control call are:

`noErr`	0	No error
`controlErr`	-17	Format failed
`wPrErr`	-44	Disk is write protected
`paramErr`	-50	Format type is out of range
`nsDrvErr`	-56	No such drive number
`noDriveErr`	-64	Drive not installed
`noNybErr`	-66	Various read errors
`badBtSlpErr`	-70	One of the address mark bit slip nibbles was incorrect (GCR)
`wrUnderRun`	-74	Write underrun occurred
`cantStepErr`	-75	Step handshake failed during seek
`initIWMErr`	-77	Unable to initialize IWM
`spdAdjErr`	-79	Unable to correctly adjust disk speed
`fmt1Err`	-82	Can’t find sector 0 after track format
`fmt2Err`	-83	Can’t get enough sync between sectors
`noIndexErr`	-83	Timed-out waiting for drive’s index pulse (MFM only)

Eject Disk

The Eject Disk control call ejects the disk in the selected drive if that drive supports removable media. Before a floppy disk is ejected, the heads will be moved to track 40 so that they will not be damaged when the disk is ejected.

The Eject Disk control call has a `csCode` of 7.

The possible result codes returned by this control call are:

`noErr`	0	No error
`nsDrvErr`	-56	No such drive number
`noDriveErr`	-64	Drive not installed
`cantStepErr`	-75	Step handshake failed during seek
`tk0BadErr`	-76	Track 0 detect doesn't change during head recalibration
`initIWMErr`	-77	Unable to initialize IWM

Set Tag Buffer

The MFM driver does not support this call. A `controlErr` (-17) is returned.

The possible result codes returned by this control call are:

`noErr`	0	No error
`controlErr`	-17	Call not available from this driver

Track Cache

When the track cache is enabled, all of the sectors on the last track accessed during a read request are read into a buffer in RAM. The sectors that were actually requested are also returned in the user's buffer. On future read requests, if the track is the same as the last track on the last read request, the sector data will be read from the cache instead of going to disk. Write requests to the driver are passed directly to the disk, and any of the sectors written that are in the cache are marked invalid.

The Track Cache control call has a `csCode` of 9.

Two bytes are passed at `csParam` to control the cache.

`csParam+0`	=0	disable the cache
	≠0	enable the cache
`csParam+1`	< 0	remove the cache; invalidate entire contents of cache (this instance in time only)
	=0	don't remove or install; no effect for MFM drives
	> 0	install the cache; invalidate entire contents of cache (this instance in time only)

The possible result codes returned by this control call are:

`noErr`	0	No error
`memFullErr`	-108	Not enough room in heap to install track cache

Return Physical Drive Icon

The Return Physical Drive Icon control call returns, at `csParam+0`, the address of an icon structure, which should contain, in this order, a 1-bit-depth icon, its mask, and a Pascal string, `Str255`, containing the information for the drive's location.

The Return Physical Drive Icon control call has a `csCode` of 21.

This information is actually obtained from the Mac OS through a low memory global, thus moving the responsibility for defining these icons to the operating system (thus, the driver does not have to know what a system enclosure looks like).

The possible result codes returned by this control call are:

`noErr`	0	No error
`controlErr`	-17	Icon does not exist or is not available
`nsDrvErr`	-56	No such drive number
`noDriveErr`	-64	Drive not installed

Return Media Icon

This call returns, at `csParam+0`, the address of an icon structure, which should contain, in the following order, a 1-bit-depth icon, its mask, and a Pascal string, `Str255`, containing the media icon location.

The Return Media Icon control call has a `csCode` of 22.

The possible result codes returned by this control call are:

`noErr`	0	No error
`controlErr`	-17	Icon does not exist or is not available
`nsDrvErr`	-56	No such drive number
`noDriveErr`	-64	Drive not installed

Return Drive Info

This control call returns a 32-bit value in `csParam` that describes the location and attributes of the selected drive.

The Return Drive Info control call has a `csCode` of 23.

The following information is returned starting at `csParam`:

`csParam +0`

Bit number	Drive type
Bits [0:3]	0 = no such drive 1 = unknown drive 2 = 400K Sony drive 3 = 400K/800K Sony drive

4 = 400K/800K/720K/1440K SuperDrive
5 = 400K/800K/720K/1440K/2880K drive
6 = 13 MB drive
7 = Apple HD-20 hard disk drive
8 through 15 = Reserved
16 = RAM disk
17 = ROM disk
18 = SLIM disk

Bits [4:7]	Reserved
Bit [8]	0 = internal drive 1 = external drive
Bit [9]	0 = floppy 1 = SCSI
Bit [10]	0 = removable media 1 = fixed media
Bit [11]	0 = primary drive 1 = secondary drive
Bits [12:31]	Reserved

The possible result codes returned by this control call are:

`noErr`	0	No error
`nsDrvErr`	-56	No such drive number
`noDriveErr`	-64	Drive not installed

Raw Track Dump

The Raw Track Dump control call reads all or part of a track and returns the raw data found there. This call gives applications access to a floppy disk at a very low level without having to directly access the disk drive controller hardware.

The Raw Track Dump control call has a `csCode` of 18244.

The following information should be passed starting at `csParam`:

`csParam+0`	`clockBitsBuffer`	pointer to packed bit array (MFM only), or nil
`csParam+4`	`dataBuffer`	pointer to raw track data, or nil
`csParam+8`	`byteCount`	number of bytes requested (the `dataBuffer` parameter must be large enough to hold this value)
`csParam+12`	`numDone`	number of bytes actually read (must be less than or equal to the `byteCount`)
`csParam+16`	`searchMode`	when to start collecting bytes: 0 = at random sector number and continue to end of track 1 = at data mark of a specified sector (one sector only) 2 = at data mark of a specified sector

(one sector only)
Codes 1 and 2 are identical for the MFM floppy disk driver
3 = at the index mark and read entire track (MFM disks only)
4 = at data mark of a specified sector (one sector only); uses the disk controller's Read Deleted Data command

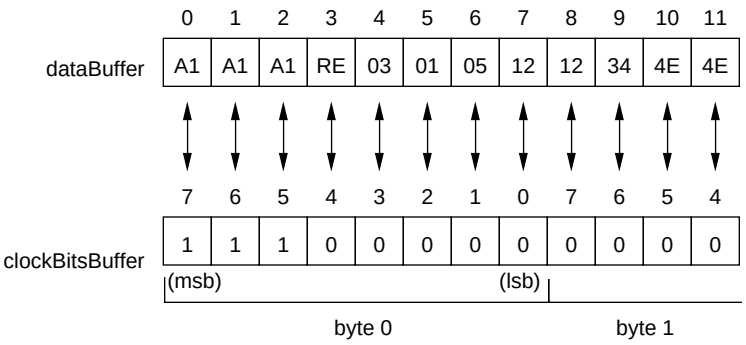
`csParam+18 track` — track to read (0-79)

`csParam+20 side` — side to read (0-1)

`csParam+21 sector` — sector to synchronize on (GCR = 0-8, 9, 10, 11; MFM = 1-9, 1-18, 1-21, etc.)
MFM sector numbers begin with a 1, unlike GCR sector numbers which begin with a 0.

`clockBitsBuffer` If a value other than nil, it points to a buffer that must be at least 1/8th the size of `dataBuffer`. this parameter consists of an array of bits signifying whether or not the corresponding byte in `dataBuffer` is a mark or data byte. If a bit is equal to "1," the byte is an MFM mark byte; if it's a "0," the byte is an MFM data byte. The relationship between bits in `clockBitsBuffer` and `dataBuffer` is shown in Figure 5-1. The example is a typical MFM address field.

Figure 5-1 Relationship between `clockBitsBuffer` and `dataBuffer`



If both `clockBitsBuffer` and `dataBuffer` are nill, the call will do nothing. This provides a way for applications to determine if the call exists without first having to allocate large buffers.

`ByteCount` This parameter specifies the number of raw bytes to read. It may not be possible to read that many bytes on every Macintosh due to differences in the way that the hardware and software are implemented, so the call will return the number of bytes that were actually read in `numDone`. If `byteCount` is zero, the call will do nothing.

`SearchMode` The parameter specifies when to begin actually collecting bytes.

In order to maintain compatibility, the MFM driver emulates the behavior of the previous Sony drivers by inserting sync and other bytes into the byte stream that is returned to the caller.

The possible result codes returned by this control call are:

`noErr`	0	No error
`controlErr`	-17	This call is not supported on the host computer
`paramErr`	-50	One or more of the parameters is out of range
`nsDrvErr`	-56	No such drive number
`noDriveErr`	-64	Drive not installed
`offLinErr`	-65	Read/write request made to an ejected disk
`noNybErr`	-66	Couldn't find 5 nibbles in 200 tries (GCR) or byte timeout (MFM)
`noAdrMkErr`	-67	Couldn't find a valid address mark
`badCkSmErr`	-69	Address mark checksum was incorrect
`badBtSlpErr`	-70	One of the address mark bit slip nibbles was incorrect (GCR)
`noDtaMkErr`	-71	Couldn't find a data mark header
`badDCkSum`	-72	Bad data mark checksum
`badDBtSlp`	-73	One of the data mark bit slip nibbles was incorrect (GCR)
`cantStepErr`	-75	Step handshake failed during seek
`twoSideErr`	-78	Tried to read a double-sided disk on a single-sided drive
`spdAdjErr`	-79	Unable to correctly adjust the drive speed (GCR, 400K drives only)
`seekErr`	-80	Wrong track number read in a sector's address field
`sectNFErr`	-81	Sector number never found on a track
`noIndexErr`	-83	Timed out waiting for index signal

DiskCopy

The DiskCopy control call performs a one-pass format and copy operation. It is useful for speeding up the disk duplication process. This call creates a RAM based version of the floppy driver when it starts up, to further increase the speed.

The DiskCopy control call has a `csCode` of 21315.

The following information should be included with the call:

`csParam+0` word length value specifies the disk format
0 = 400K GCR
1 = 800K GCR
2 = 720K MFM
1 = 1440K MFM (high density media)
1 = 2880K MFM (extended density media)
2 = 1680K DMF MFM (high density media)

`csParam+2` this long integer value is a pointer to a buffer containing the data from all the sectors on the disk

`csParam+6` this long integer value is a pointer to a buffer containing all the tags from all the sectors on the disk

`csParam+10` this byte value defines the format byte for GCR disks
0x12 = Macintosh 400K
0x22 = Macintosh 800K
0x24 = Apple II 800K
this field is ignored for the MFM disk format

`csParam+11` if a nonzero value, verify that the data was written out correctly

Since the MFM drive controller is incapable of performing a format and write in one operation, this call is implemented by simply calling the internal Format, Write, and Read-Verify routines, very much as if the client had made these calls in sequence.

IMPORTANT

Version 1.0 of the MFM floppy disk driver does not support the copying of DMF MFM format disks. It may be implemented in a future version of the driver. ▲

The definitions for result codes returned by the DiskCopy control call are:

`noErr`	0	No error
`controlErr`	-17	This call is not supported on the host
`wPrErr`	-44	Disk is write protected
`paramErr`	-50	One or more of the parameters is out of range
`nsDrvErr`	-56	No such drive number
`noDriveErr`	-64	Drive not installed
`offLinErr`	-65	Read/write request made to an ejected disk
`noNybErr`	-66	Couldn't find 5 nibbles in 200 tries (GCR) or byte timeout (MFM)
`noAdrMkErr`	-67	Couldn't find a valid address mark
`dataVerErr`	-68	Read verify compare failed
`badCkSmErr`	-69	Address mark checksum was incorrect
`badBtSlpErr`	-70	One of the address mark bit slip nibbles was incorrect (GCR)
`noDtaMkErr`	-71	Couldn't find a data mark header
`badDCkSum`	-72	Bad data mark checksum
`badDBtSlp`	-73	One of the data mark bit slip nibbles was incorrect (GCR)
`wrUnderRun`	-74	Couldn't write fast enough to keep up with the IWM
`cantStepErr`	-75	Step handshake failed during seek
`tk0BadErr`	-76	Track 0 detect sensor doesn't change during a head recalibration
`initIWMErr`	-77	Unable to initialize IWM
`twoSideErr`	-78	Tried to read a double-sided disk on a single-sided drive
`spdAdjErr`	-79	Unable to correctly adjust the drive speed (GCR, 400K drives only)
`seekErr`	-80	Wrong track number read in a sector's address field
`sectNFErr`	-81	Sector number never found on a track
`fmt1Err`	-82	Can't find sector 0 after track format
`fmt2Err`	-83	Can't get enough sync between sectors
`noIndexErr`	-83	Timed out waiting for drive's index pulse (MFM only)

Enable Close

The standard behavior of the Close control call is to perform no function. The Enable Close control call makes the Close call fully operational.

The Enable Close control call has a `csCode` of 16971.

If Close is called after Enable Close has been called, the Close control call deallocates all memory and other driver resources, and returns `noErr`.

The Enable Close control call has no parameters or errors.

Close

The Close control call performs no operation on the drive and returns `closErr`. This is not the case however when the Enable Close call is made after the driver is opened and prior to calling the Close call. See the description of the Enable Close call.

Status Calls

As with the control calls, the status opcode is passed to the driver in the `csCode` field of the I/O parameter block (byte 26). The returned status information is passed back starting at the `csParam` field of the I/O parameter block (byte 28).

Return Format List

This call returns a list of all possible disk formats available with the current combination of disk controller, drive, and media.

The Return Format List status call has a `csCode` of 6.

On entry, `csParam+0` contains a value specifying the maximum number of formats to return, and `csParam+2` contains a pointer to a table that contains the list.

On exit, `csParam+0` contains the number of formats returned (no more than specified), and the table contains the list of formats. If no disk is inserted in the drive, the call returns a `noDriveErr` result code. The format information is given in an 8-byte record as follows:

```
Tuple+0  long32:  number of 512-byte sized blocks
Tuple+1  long32:  Bits[0:15] number of cylinders (0-65535)
                  Bits[16:23] number of sectors per track
                  Bits[24:27] number of sides (heads) per cylinder
                              (0-15)
                  Bit[28]  0 = single density, 1 = double density
```

```
Bit[29]  0 = able to format in this format
         1 = unable to format in this format
Bit[30]  0 = current disk has this format
         1 = does not have this format
Bit[31]  0 = support variable cylinder/sectors
         1 = does not support variable
             cylinder/sectors
```

The list that is returned changes depending on the type of media (low density/high density, and so on.) is currently inserted. If no media is inserted, an error is returned.

Bit [29] (unable to do FormatDisk in this format) is new for this driver and is intended to notify applications that the driver can read (and maybe in the future write) DMF, but cannot format a disk with DMF.

The possible result codes returned by this status call are:

`noErr`	0	No error
`controlErr`	-17	This call is not supported on the host computer
`paramErr`	-50	One or more of the parameters is out of range
`nsDrvErr`	-56	No such drive number
`noDriveErr`	-64	Drive not installed

Drive Status

The Drive Status status call returns information about a particular drive.

The Drive Status status call has a `csCode` of 8.

The following information is returned by the Drive Status call:

`csParam+0` this word value indicates the current track

`csParam+2` if bit 7 in this byte is set, the disk is write protected

`csParam+3` this byte value is defined as:
<0 = disk is being ejected
0 = no disk is currently in the drive
1 = disk was just inserted, but no read/write requests have been made yet
2 = operating system has tried to mount the disk (a read request to driver)
3 = same as 2, except that the disk is a high-density formatted as 400K/800K GCR

`csParam+4` this byte is defined as:
-1 = no drive installed
0 = don't know
1 = drive installed

`csParam+5` this byte indicates the number of sides
0 = single-sided, -1 = double-sided

`csParam+6` this long integer value is a pointer to the next drive queue element

`csParam+10` this word value indicates the type of queue (`drvQType`)

`csParam+12` this word value specifies the drive number

`csParam+16` this word value defines the driver reference number

`csParam+18` this byte value specifies the file system ID

`csParam+19` this byte value specifies the current format
0 = current disk is single-sided format
1 = current disk is double-sided format

`csParam+20` this word value contains the soft error count for the disk

The definitions for the possible result codes returned by this call are:

`noErr`	0	No error
`controlErr`	-17	This call is not supported on the host computer
`nsDrvErr`	-56	No such drive (bad `ioVRefNum`)

MFM Status

The MFM Status status call only exists in versions of the driver that support MFM disks. By making this call and then checking the returned error code, it is possible to determine whether or not the current driver can read and write MFM disks. Also, the information returned is helpful in determining the installed hardware configuration.

The MFM Status status call has a `csCode` of 10.

The following information is returned by the MFM Status call:

`csParam+0` drive type
0 = 400K/800K GCR
-1 = SuperDrive (MFM/GCR)

`csParam+1` disk format
0 = GCR
-1 = MFM

`csParam+2` MFM format
1 = unknown or no disk
0 = 720K
-1 = 1440K
-2 = 2880K
-3 = DFM format (1680K)

`csParam+3` floppy disk controller
0 = IWM
-1 = SWIM
-2 = SWIM2
-3 = NewAge FDC
-4 = SWIM3
-5 = Intel standard FDC37C78

The definitions for the possible result codes returned by this call are:

`noErr`	0	No error
`controlErr`	-17	This call is not supported on the host
`nsDrvErr`	-56	No such drive installed (bad `ioVRefNum`)

DiskCopy Version Status

The DiskCopy Version Status status call returns the version of the duplicator supported by the current floppy disk driver.

The DiskCopy Version Status status call has a `csCode` of 17494.

The version number is returned in `csParam`. Currently that value is 0x0410.

The definitions for the possible result codes returned by this call are:

`noErr`	0	No error
`controlErr`	-17	This call is not supported on the host
`nsDrvErr`	-56	No such drive installed (bad `ioVRefNum`)

Last Format Byte

The Last Format Byte status call returns the last format byte read. The byte is located in each sector address field on the disk and contains the format and interleave.

The Last Format Byte status call has a `csCode` of 21315.

The information returned in `csParam` is as follows:

`csParam+0` 0x02 = 720K, 1440K, and 2880K MFM
0x12 = 400K GCR
0x22 = 800K GCR
0x24 = Apple II 800K GCR

The definitions for the possible result codes returned by this call are:

`noErr`	0	No error
`controlErr`	-17	This call is not supported on the host

Copy Protection and MFM Floppy Disk Controllers

The MFM floppy drive controller hardware does not allow a Track Dump control call to be implemented in the way it was implemented with GCR floppy drive controllers. The MFM driver supports a Raw Track Dump call, which is an emulated Track Dump call. Copy protection schemes that use the Track Dump call to perform floppy disk copy protection will fail to work correctly, because the emulated version of the Track Dump

control call for MFM does not read the track including the actual intertrack data and sync bytes.

The MFM floppy disk controller does not support a FormatWrite operation. With the MFM floppy disk controller the DiskCopy control call is implemented as three separate driver calls, a Format, a Write, and a Verify. These calls do not perform such explicit checking as to whether or not sectors end up in the same relative locations between adjacent tracts. Therefore, copies are not exact duplicates and copying copy-protected floppy disks is not possible.

Previously, copying copy-protected floppy disks was possible with GCR controllers by making a call to the DiskCopy control call. The DiskCopy control call requested the floppy disk controller to perform a FormatWrite operation, which was capable of performing a one-pass format and write operation for an entire track and cylinder at a time. This allowed copying of disks without regard for inter-track sector alignment and other copy protection attributes. The result was always an exact duplicate.

Floppy Drive Gestalt Selector

A floppy drive gestalt selector is defined to provide high-level applications a way to determine some of the basic attributes of the floppy drive installed in a system. The gestalt value is `'flpy'`. The floppy drive selector returns 32 bits. The three least significant bits are used to indicate what type of drive is installed.

Bit numbers 0 through 2 are true/false switches for the floppy disk drive attributes described in Table 5-2.

Table 5-2 Floppy disk drive attributes bit values

Bit	Description
0	Floppy drive only does MFM disk formats.
1	Floppy disk drive, driver, file system in manual-eject mode.
2	Floppy disk drive has special DISK-IN-PLACE output; standard DISK-CHANGED output signal from drive is not used.

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