Developer Note

# Power Mac G4 Computer

July 2000

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Simultaneously published in the United States and Canada.

# Contents

# Figures and Tables

# About This Note

This developer note describes the Power Mac G4 computer. The note provides information about the internal design of the computer, its input-output and expansion capabilities, and issues affecting compatibility.

**Note**
This developer note has been updated to include information about the latest product configurations. ◆

This developer note is intended to help hardware and software developers design products that are compatible with the Macintosh products described here. If you are not already familiar with Macintosh computers or if you would simply like additional technical information, you should refer to Appendix A, "Supplemental Reference Documents,"

The information is arranged in four chapters:

- Chapter 1, "Introduction," gives a summary of the features of the Power Mac G4 computer, describes the physical appearance of the enclosure, and lists compatibility issues of interest to developers.
- Chapter 2, "Architecture," describes the internal organization of the computer. It includes a functional block diagram and descriptions of the main components on the logic board.
- Chapter 3, "Input and Output Devices," describes the built-in I/O devices and the external I/O ports.
- Chapter 4, "Expansion," describes the expansion slots on the logic board and provides specifications for the expansion modules.

CHAPTER 1

# Introduction

The Power Mac G4 computer is the latest Macintosh desktop computer using the PowerPC G4 microprocessor. It is intended for use in content creation, desktop publishing, multimedia, and other activities that require high performance.

## New Features

The Power Mac G4 computer is an enhanced version of the Power Mac G4 computer. Many of its features are the same as those of the earlier machine. Here is a list of the new features.

- **Dual processors:** Some configurations of the Power Mac G4 have two microprocessors operating in parallel. For information about software and dual processors, see "Dual Processor Support" (page 16).
- **1000Base-T Ethernet:** The built-in Ethernet port supports 1000Base-T operation. See "Ethernet Port" (page 39)
- **Keyboard:** The computer comes with an Apple Pro Keyboard, a full-size USB keyboard. For more information, see "Keyboard" (page 46).
- **Mouse:** The computer comes with an Apple Pro Mouse, a USB mouse with optical tracking. For more information, see "Mouse" (page 49).

## Hardware Features

Here is a list of the hardware features of the Power Mac G4 computer. The major features are described more fully later in this note.

- **Microprocessor:** PowerPC G4 microprocessor running at a clock frequency of 400, 450, or 500 MHz depending on model and configuration. For more information, see "PowerPC G4 Microprocessor" (page 22).
- **Dual processors:** Some configurations of the Power Mac G4 have dual processors. For information about software and multiprocessing, see "Dual Processor Support" (page 16).
- **Cache:** 1 MB of backside L2 cache for each processor. The cache runs at half the clock frequency of the microprocessor(s).

- **Processor system bus:** 64-bit wide data and 32-bit wide address, 100 MHz clock, supporting MaxBus protocol. For more information, see "Processor Bus" (page 23).
- **RAM:** Four DIMM slots for 168-pin PC100 DIMMs (dual inline memory modules) using SDRAM (synchronous dynamic access memory) or ESDRAM (enhanced SDRAM) devices. A minimum of 64 MB of RAM is installed in one of the slots. For more information, see "RAM Expansion" (page 58).
- **ROM:** ROM-in-RAM implementation with 1 MB of boot ROM. For information about the ROM, see "Boot ROM" (page 25). For information about the ROM-in-RAM implementation, see the references listed in "ROM-in-RAM Architecture" (page 67).
- **Graphics acceleration:** A graphics card in the AGP slot provides 2D and 3D hardware graphics acceleration using the ATI RAGE 128 Pro graphics controller. For more information, see "AGP Graphics Card" (page 29).
- **Sound:** Support for 16 bits/channel stereo input and output on built-in 3.5 mm line-level stereo input and output jacks and one built-in speaker. For more information, see "Sound System" (page 49).
- **Hard disks:** One internal Ultra DMA/66 hard disk; provision for adding either a second Ultra DMA/66 disk or an ATA-3 storage device. For more information, see "Ultra DMA/66 Hard Disk" (page 41).
- **Drive bays:** Three drive bays, one of which is occupied by an Ultra DMA/66 hard disk. Two bays are available for adding one internal 3.5 x 1-inch Ultra DMA/66 or two ATA-3 devices, or other devices connected to a PCI controller card. An Ultra SCSI 160 drive and Ultra SCSI 160 PCI controller card are available as a configuration option. For more information, see "Disk Drives" (page 41).
- **DVD-ROM drive:** ATAPI **8x**-speed DVD-ROM drive. It also reads 24x-speed CD-ROM media and provides DVD-Video playback with DVD MPEG2 decode in software. For more information, see "DVD-ROM Drive" (page 42).
- **DVD-RAM drive:** Optional ATAPI DVD-RAM drive reads and writes 2.6 GB and 5.2 GB DVD-RAM media; it also supports 6x-speed DVD-ROM, 20x CD-ROM, and DVD-Video playback with DVD MPEG2 decode in software. For more information, see "DVD-RAM Drive" (page 42).

- **Zip drive:** All configurations can accept an optional 100 MB ATAPI Zip drive. For more information, see "Optional Zip Drive" (page 43).
- **USB ports:** Two USB ports, described in "USB Ports" (page 34). The keyboard that comes with the computer has two additional USB ports.
- **Ethernet:** Built in Ethernet port with an RJ-45 connector for 10Base-T, 100Base-T, or 1000Base-T operation on all configurations. For more information, see "Ethernet Port" (page 39).
- **Wireless LAN:** An internal wireless LAN module is available as a build-to-order option or as a user-installable upgrade. For more information, see "AirPort Card Wireless LAN Module" (page 44).
- **FireWire ports:** Two external IEEE 1394 high-speed serial FireWire ports, with transfer rates of 100, 200, and 400 Mbps and support for booting from a FireWire storage device. For more information, see "FireWire Ports" (page 36).
- **Modem:** Slot for an optional built-in Apple 56 Kbps modem. The modem supports K56flex and V.90 modem standards. For more information, see "Internal Modem" (page 44).
- **Keyboard:** The computer comes with an Apple Pro Keyboard, a full-size USB keyboard. The keyboard is also a bus-powered USB hub with two USB ports. For more information, see "Keyboard" (page 46).
- **Mouse:** The computer comes with an Apple Pro Mouse, a USB mouse with optical tracking. For more information, see "Mouse" (page 49).
- **PCI card expansion slots:** Three slots for 33 MHz, 64-bit or 32-bit, 12-inch PCI cards. For more information, see "PCI Expansion Slots" (page 62).
- **AGP-2X graphics card slot:** The computer is always shipped with an accelerated graphics card installed in this slot. For more information, see "AGP Graphics Card" (page 29).
- **Voltage switch:** Can be set to either 115 for voltages of 100–130 V or 230 for voltages of 200–250 V, depending on the voltage where the computer is installed. The voltage selection must be set manually.
- **Fan speed control:** The speed of the fan is thermally controlled and is automatically set to the lowest possible speed to minimize noise. This is a function provided by the fan and is not under software control.
- **Energy saving:** Sleep, startup, and shutdown scheduling can be controlled with an Energy Saver control panel.

# Features of the Enclosure

The Power Mac G4 computer's enclosure is a mini-tower design with opaque side panels and transparent handles.

The front of the computer's enclosure has the slots for the DVD-ROM or DVD-RAM drive and the optional Zip drive, three buttons—power, reset, and NMI—and the power-on light.

The back panel includes the A/C power socket, the monitor power socket, the I/O ports, and the openings for PCI cards.

The user can get access to the main logic board to add memory or PCI cards by opening the case and swinging the door down.

# System Software

The Power Mac G4 computer comes with Mac OS 9 installed. For the latest information about Mac OS 9, see the references listed in "Mac OS 9" (page 67).

## ROM In RAM

Since the introduction of the first iMac model, Macintosh system software has used a design based on ROM in RAM and Open Firmware. With this approach, a small ROM contains the code needed to initialize the hardware and load an operating system. The rest of the system code that formerly resided in the Mac OS ROM is loaded into RAM from disk or from the network. For more information, see the references listed in "ROM-in-RAM Architecture" (page 67) and "Open Firmware" (page 68).

## Computer Identification

Rather than reading the box flag or the model string and then making assumptions about the computer's features, applications that need to find out the features of the machine should use Gestalt calls to test for the features they require.

Asset management software that reports the kind of machine it is run on can obtain the value of the property at `Devices:device-tree:compatible` in the name registry. The model string is the first program-usable string in the array of C strings in the `compatible` field. For the Power Mac G4, the value of the model property is `PowerMac3,3`.

The string obtained from the `compatible` property cannot be displayed to the computer user. A better method, if it is available, is to use the result from calling `Gestalt ('mnam', &result)` where `result` is a string pointer. This call returns a Pascal-style string that can be displayed to the user.

## Dual Processor Support

The system software includes Multiprocessing Services, an API that allows your application to create tasks that run independently on one or more processors.

**IMPORTANT**

To gain a performance advantage on dual-processor configurations, applications must be modified to use Multiprocessing Services. ▲

Multiprocessing Services allows you to create preemptive tasks within an application. The application still operates in a cooperative multitasking environment with respect to other applications.

Multiple processor support is transparent in Multiprocessing Services. If multiple processors are available, Multiprocessing Services divides the tasks among the available processors. If only one processor is available, Multiprocessing Services schedules all the tasks with that processor.

Multiprocessing Services allows you to determine the number of processors available before creating any tasks.

To obtain more information, including interfaces and libraries, documentation, demonstration applications, and sample code, refer to the references in “Multiprocessing Services” (page 66).

## CPU Power Modes

The current Power Manager, version 2.0, is a native Mac OS manager designed to implement a common power management strategy across all Macintosh models. Under Power Manager 2.0 on the Prototype 15, the following states are defined:

- **Run Multiple:** The system is running at maximum processing capacity. In a single processor system the processor is running at full speed. In a multi-processor system all processors are running at full speed.
- **Run Single:** One processor is running at maximum processing capacity. In a single processor system, this is the same as Run Multiple. In a multi-processor system, only one processor is running at full speed; all other processors are in sleep mode with their caches flushed and their states saved.
- **Idle One:** The system is idling. All clocks are running and the system can return to running code within a few nanoseconds. In a single processor system, the main processor is stopped in Doze mode. Cache coherency is maintained in this level of idle. In a multi-processor system, all other processors will be sleeping as described in Run Single.
- **Idle Two:** The system is in power saving mode. This mode is entered only when a system has been in Idle One state for a substantial period of time (a half second or so) with no activity. In a single processor system, the main processor cache is flushed, and the processor is put into sleep mode—the external processor bus clock is stopped. The delay in coming out of this state is on the order of a millisecond. Cache coherency is maintained by the flush on entry. In a multi-processor system, the other processors will be sleeping as described in Run Single.
- **Doze:** The power to the disk drive motors and the display is turned off, but the power supply and fan are still on. The computer can still respond to network activity.
- **Sleep:** The system is completely shut down, with only the DRAM state preserved for quick recovery. All processors are powered off with their state preserved in DRAM. All clocks in the system are suspended except for the 32.768Khz timebase crystal on the PMU99 IC. This mode allows desktop systems to meet 5W sleep requirements while providing the ability to start up without rebooting.

## Velocity Engine Acceleration

The Velocity Engine (also called AltiVec) is a vector processing unit that is new with the G4 microprocessor. Some system software has been modified to take advantage of the accelerated processing that it makes possible. System software has also been modified to support low-level operations using the Velocity Engine.

The software areas that have been modified to take advantage of Velocity Engine acceleration are

- QuickTime: key codecs, including DV and photo JPEG

The software areas that have been added or modified for low-level Velocity Engine support are

- Nanokernel: the floating-point vector denormal handler
- Process Manager: context switching
- Block Move routines

The following vector libraries are included: vBasicOps, vectorOps, vBigNum, and vMathLib.

CHAPTER 2

# Architecture

This chapter describes the architecture of the Power Mac G4 computer. It includes information about the major components on the logic boards: the microprocessor, the other main ICs, and the buses that connect them to each other and to the I/O interfaces.

# Block Diagram and Buses

Figure 2-1 is a simplified block diagram of the Power Mac G4 computer. The diagram shows the main ICs and the buses that connect them together.

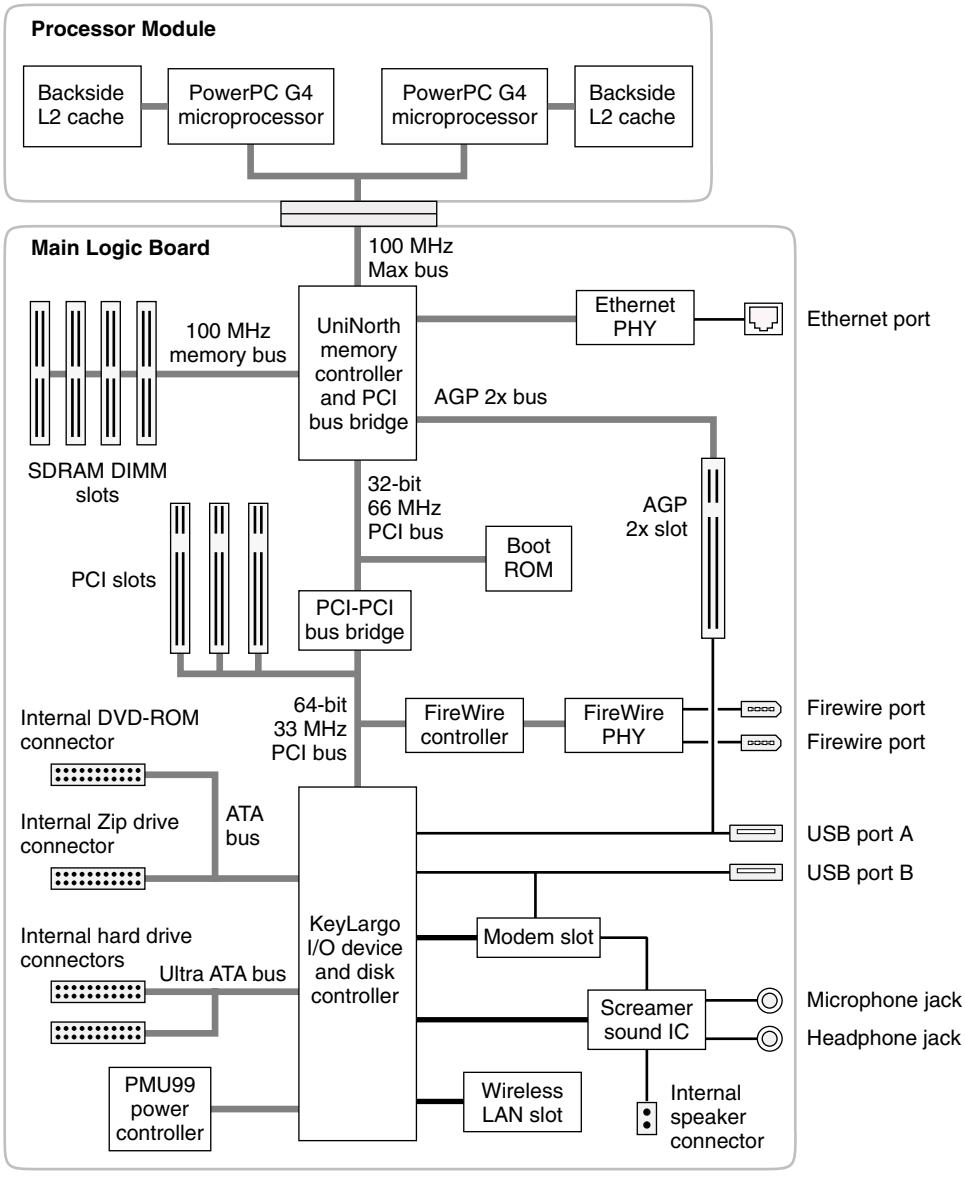
The architecture of the Power Mac G4 is based on the PowerPC G4 microprocessor and two custom ICs: the Uni-N memory controller and bus bridge, and the KeyLargo I/O controller.

The Power Mac G4 has four separate buses, not counting the processor's dedicated interface to the backside cache.

- **Processor bus:** 100-MHz, 64-bit bus connecting the processor module to the Uni-N IC
- **Memory bus:** 100-MHz, 64-bit bus connecting the main memory to the Uni-N IC
- **AGP bus:** 66 or 132-MHz, 32-bit bus connecting the AGP graphics card to the Uni-N IC
- **PCI bus:** 66-MHz, 32-bit bus connecting the boot ROM and the PCI-PCI bridge IC to the Uni-N IC; 33-MHz, 64-bit bus connecting the KeyLargo I/O controller and the PCI slots to the PCI-PCI bridge IC

The remainder of this chapter describes the architecture in three parts centered around the processor module, the Uni-N memory controller and bridge IC, and the KeyLargo I/O controller IC.

**Figure 2-1** Simplified block diagram



# Processor Module

The processor module is a separate logic board that contains one or two G4 microprocessors and their backside L2 caches.

The processor module is connected to the main logic board by way of a 300-pin connector. To achieve the required level of performance, the signal lines that connect the processor module and the main logic board are carefully matched in length, loading, and impedance.

## PowerPC G4 Microprocessor

The PowerPC G4 microprocessor used in the Power Mac G4 computer has many powerful features, including a new pipelined system bus that is more efficient than the system bus on the PowerPC G3 microprocessors. The new bus design, called MaxBus, allows for much greater efficiency of bus utilization than was possible with the previous design.

Features of the PowerPC G4 include:

- 32-bit PowerPC implementation
- superscalar PowerPC core
- Velocity Engine (AltiVec technology): 128-bit-wide vector execution unit
- dual 32 KB instruction and data caches (the same as PowerPC G3)
- support for up to 2 MB backside L2 cache
- on-chip L2 tag storage (twice as much as PowerPC G3)
- high bandwidth MaxBus (also compatible with 60x bus)
- fully symmetric multiprocessing capability

To find more information, use the links at “PowerPC G4 Microprocessor” (page 65).

### Level2 Cache

Each backside level2 (L2) cache consists of 1 MB of high-speed SRAM. The clock frequency of the L2 cache is half the clock frequency of the PowerPC G4 microprocessor.

**Note**
The Power Mac G4 computer does not use jumpers to control the clock speeds of the processor and cache. ◆

### Dual Processors

Some configurations of the Power Mac G4 have a processor card that contains two Power PC G4 processors, each with its own 1-MB L2 cache. The dual-processor configuration allows applications that support multitasking to double their performance. For more information, see “Dual Processor Support” (page 16).

## Uni-N Bridge and Memory Controller

The Uni-N custom IC is at the heart of the Power Mac G4 computer. It provides the bridging functionality between the processor, the memory system, the PCI-based I/O system, the AGP graphics slot, and the Ethernet interface.

### Processor Bus

The processor bus is a 100-MHz, 64-bit bus connecting the processor module to the Uni-N IC. In addition to the increased bus clock speed, the bus uses MaxBus protocols, supported by the Uni-N IC, for improved performance.

The MaxBus protocol includes enhancements that improve bus efficiency and throughput over the 60x bus. The enhancements include

- out of order completion
- address bus streaming
- intervention

Out of order completion allows the memory controller to optimize the data bus efficiency by transferring whichever data is ready, rather than having to pass data across the bus in the order the transactions were posted on the bus. This means that a fast DRAM read can pass a slow PCI read, potentially enabling the processor to do more before it has to wait on the PCI data.

Address bus streaming allows a single master on the bus to issue multiple address transactions back-to-back. This means that a single master can post addresses at the rate of one every two clocks, as opposed to one every three clocks, as it is in the 60x bus protocol.

Intervention is a cache coherency optimization that improves performance for dual processor systems. If one processor modifies some data, that data first gets stored only in that processor's cache. If the other processor then wants that data, it needs to get the new modified values. In previous systems, the first processor must write the modified data to memory and then the second processor can read the correct values from memory. With intervention, the first processor sends the data directly to the second processor, reducing latency by a factor of ten or more.

## Main Memory Bus

The main memory bus is a 100-MHz, 64-bit bus connecting the main memory to the Uni-N IC.

Main memory is provided by up to four PC100 DIMMs. Supported DIMM sizes are 16, 32, 64, 128, 256, and 512 MB. Although the memory slots will accept four 512-MB DIMMs, the maximum memory size supported by Mac OS 9 is 1.5 GB.

For more information about memory DIMMs, see "RAM Expansion" (page 58).

## Accelerated Graphics Port Bus

The accelerated graphics port (AGP) bus is a 66 or 132-MHz, 32-bit bus connecting the AGP graphics card to the Uni-N IC. The AGP bus provides faster access to main memory than previous designs using the PCI bus.

The AGP bus is a superset of the PCI bus, but it has separate address lines so it does not multiplex address and data as PCI does. Having a separate address bus allows the AGP bus to pipeline addresses, thereby improving performance.

To further improve the performance of the AGP bus, the Uni-N IC supports a graphics address remapping table (GART). Because the virtual memory system

organizes main memory as randomly distributed 4 KB pages, DMA transactions for more than 4 KB of data must perform scatter-gather operations. To avoid this necessity for AGP transactions, the GART is used by the AGP bridge in the Uni-N to translate a linear address space for AGP transactions into physical addresses in main memory.

## PCI Buses and Bridge

The Power Mac G4 has two PCI buses. The first PCI bus is a 66-MHz, 32-bit bus from the Uni-N IC. The second PCI bus is a 33-MHz, 64-bit bus to the KeyLargo I/O controller and the PCI slots. The PCI-PCI bridge IC provides the conversion between the two PCI buses. The rationale behind this arrangement has to do with reducing the number of pins on the Uni-N IC.

The PCI-to-PCI bridge IC is a DEC 21154-66 device. In addition to bridging between the two PCI buses, it provides performance enhancing features such as write buffering, memory read-ahead buffering, and transaction optimization.

The PCI-to-PCI bridge IC also provides arbitration for the 33 MHz secondary PCI bus. This arbiter is a two-tier round-robin arbiter. The low-priority tier gets one slot in the high-priority round-robin arbitration scheme. Placement of devices in the arbitration scheme is under software control, so any device may be placed in either the high-priority tier or the low-priority tier. For more details of the arbiter, see the DEC 21154-66 databook.

## Boot ROM

The boot ROM consists of 1 MB of on-board flash EPROM. The boot ROM includes the hardware-specific code and tables needed to start up the computer, to load an operating system, and to provide common hardware access services.

To minimize the number of pins on Uni-N, the boot ROM is connected to the 66 MHz PCI bus. The boot ROM uses the thirty two PCI AD lines and four PCI byte enable lines for address and data. Uni-N has separate pins for Chip Enable, Output Enable, and Write Enable signals to keep the ROM from interfering with proper PCI bus operation.

## Ethernet Controller

The Uni-N IC includes an Ethernet media access controller (MAC). As a separate I/O channel on the Uni-N IC, it can operate at its full capacity without

degrading the performance of other peripheral devices. The Uni-N IC provides DB-DMA support for the Ethernet interface.

The MAC implements the link layer. It is connected to a pair of PHY interface ICs: one operates in 10-BaseT mode, the other in 100-BaseT or 1000-BaseT mode. The operating speed of the link is automatically negotiated by the PHY ICs and the bridge or router to which the port is connected. For information about the port, see "Ethernet Port" (page 39).

### FireWire Controller

The PCI bus supports an IEEE 1394 FireWire controller IC with a maximum data rate of 400 Mbits (50 MBytes) per second. The controller IC implements the FireWire link layer. A physical layer IC, called a PHY, implements the electrical signaling protocol of the FireWire interface. The PHY supports two FireWire ports by way of the external connectors on the rear panel.

The computer is capable of accepting external power through the FireWire connector to operate the PHY when the computer is turned off. While the PHY is operating, it acts as a repeater from one port to another so that the FireWire bus remains connected. For more information, see "FireWire Ports" (page 36).

## KeyLargo I/O Controller

The KeyLargo custom IC is the third major component of the architecture. It provides all the I/O functions except Ethernet and FireWire. The KeyLargo IC provides two USB root hubs, an Ultra DMA/66 interface, an EIDE interface, and support for the communication slot and the sound IC.

### DMA Support

The KeyLargo IC provides DB-DMA (descriptor-based direct memory access) support for the following I/O channels:

- Ultra DMA/66 interface
- EIDE interface

- communication slot interface
- DAV channel to the sound IC

The DB DMA system provides a scatter-gather process based on memory-resident data structures that describe the data transfers. The DMA engine is enhanced to allow bursting of data files for improved performance.

## Interrupt Support

The interrupt controller for the Power Mac G4 system is an MPIC cell in the KeyLargo IC. In addition to accepting all the KeyLargo internal interrupt sources, the MPIC controller accepts external interrupts from dedicated interrupt pins and serial interrupts from the Uni-N serial interrupt stream. The signals from the Uni-N IC are synchronized to the operation of the MPIC circuitry, so there is no additional interrupt latency on the Uni-N interrupts.

## USB Interface

The KeyLargo IC implements two independent USB root hubs, each of which is connected to one of the ports on the back panel of the computer. The use of two independent hubs allows both USB ports to support high data rate devices at the same time with no degradation of their performance. If a user connects a high-speed device to one port and another high-speed device to the other, both devices can operate at their full data rates.

The two external USB connectors support USB devices with data transfer rates of 1.5 Mbps or 12 Mbps. For more information, see “USB Ports” (page 34).

Internally, the second port of one controller is routed to the USB signal pair on the AGP slot. The second port of the other controller is routed to the modem slot for an internal USB modem.

The USB ports comply with the Universal Serial Bus Specification 1.0 Final Draft Revision. The USB register set complies with the Open Host Controller Interface (OHCI) specification.

## Ultra DMA/66 Interface

The KeyLargo IC implements a single Ultra DMA/66 hard disk interface. This interface supports the boot drive and can accommodate a second hard drive.

The KeyLargo IC provides DB-DMA (descriptor-based direct memory access) support for the Ultra DMA/66 interface.

## Enhanced IDE Interface

In the Power Mac G4, the KeyLargo IC provides an enhanced IDE (EIDE) interface. The EIDE interface supports the DVD drive and an optional Iomega Zip removable media drive.

The KeyLargo IC provides DB-DMA (descriptor-based direct memory access) support for the EIDE interface.

## Modem Slot Support

The KeyLargo IC has a traditional Macintosh serial port that is connected to the modem slot. The KeyLargo IC also provides digital audio to the slot in the form of an $I^2S$ port that shares pins with the serial port.

The KeyLargo IC provides DB-DMA (descriptor-based direct memory access) support for the modem slot interface.

The internal hardware modem is a separate module that contains a modem controller IC, a datapump, and the interface to the telephone line (DAA). For more information about the modem, see “Internal Modem” (page 44).

## Wireless LAN Module

The interface between the wireless LAN module and the KeyLargo IC is similar to a PC Card interface.

The AirPort Card wireless LAN module contains a media access controller (MAC), a digital signal processor (DSP), and a radio-frequency (RF) section. The module has a connector for the cable to the antennas, which are built into the computer’s case.

The wireless LAN module is based on the IEEE 802.11 standard. The wireless LAN module transmits and receives data at up to 11 Mbps and is compatible

with older systems that operate at 1 or 2 Mbps. For information about its operation, see “AirPort Card Wireless LAN Module” (page 44).

## Sound IC Support

The KeyLargo IC has a traditional DAV port that connects to the Screamer sound IC. The KeyLargo IC provides DB-DMA (descriptor-based direct memory access) support for the DAV port.

The Screamer sound IC is an audio codec with added input and output controls. It is a 16-bit device with two analog stereo input channels and two analog stereo output channels. Either stereo pair of input channels can be selected for digitization by the internal A-to-D converter.

Audio data from the CD-ROM drive are sent through the KeyLargo IC’s DMA channel and then to the Screamer IC for conversion to analog signals.

For a description of the features of the sound system, see “Sound System” (page 49).

## Power Controller

The power management controller in the Power Mac G4 is a custom IC called the PMU99. It supports new modes of power management that provide significantly lower power consumption than previous systems. For more information, see “CPU Power Modes” (page 17).

# AGP Graphics Card

The computer comes with an AGP graphics card installed. The graphics card has the following specifications:

- ATI’s RAGE 128 PRO graphics IC
- 16 MB SDRAM on a 128-bit, 125-MHz SDRAM bus
- Apple display connector (ADC) for a digital monitor
- support for up to 1600 by 1024 pixels on a digital monitor

- 3-row mini DB-9/15 (VGA) connector for an analog video monitor
- support for up to 1920 by 1200 pixels on an analog monitor

For more information about the features of the graphics card and the monitors it supports, see "Video Monitor Ports" (page 51).

## Graphics Controller IC

The ATI RAGE 128 PRO graphics controller IC on the accelerated graphics card contains the logic for the video display. The ATI RAGE 128 PRO graphics controller includes the following features:

- advanced 128-bit rendering engine
- architecture optimized to support high-speed SDRAM video memory
- display memory controller, built-in drawing coprocessor, video scaler, color space converter, clock generator, and true color palette video DAC (digital-to-analog converter)
- video CLUT (color lookup table)
- integrated support for digital flat panel monitors
- hardware graphics acceleration with a 16-bit Z-buffer
- accelerated QuickDraw 3D rendering up to six times that of software-only acceleration
- true color palette DAC supporting pixel clock rates to 250 MHz
- graphics and video line buffer for superior video scaling and playback quality
- hardware cursor up to 64 x 64 x 2
- DDC1 and DDC2B+ for plug-and-play monitor support
- graphics control accessible through the QuickDraw, QuickDraw 3D, QuickDraw 3D RAVE, and QuickTime components APIs

A separate data bus handles data transfers between the ATI RAGE 128 PRO graphics controller and the display memory. The display memory data bus is 128 bits wide, and all data transfers consist of 128 bits at a time. The RAGE 128 PRO IC breaks each 128-bit data transfer into several pixels of the appropriate size for the current display mode—4, 8, 16, 24, or 32 bits per pixel.

The ATI RAGE 128 PRO graphics controller uses several clocks. Its transactions are synchronized with the AGP bus. Data transfers from the frame-buffer RAM are clocked by the MEM_CLK signal. Data transfers to the CLUT and the video output are clocked by the dot clock, which has a different rate for different display monitors.

The 2D graphics accelerator is a fixed-function accelerator for rectangle fill, line draw, polygon fill, panning/scrolling, bit masking, monochrome expansion, and scissoring.

## Display Memory

The display memory on the AGP graphics card is separate from the main memory. The display memory consists of 16 MB of 140 MHz SDRAM devices configured to make a 128-bit data bus. The display memory cannot be expanded by the user.

The graphics card has 16 MB of video memory, allowing the analog monitor display to have pixel depths of 8, 16, or 32 bpp for displays up to 1280 by 1024 pixels and 8 or 16 bpp for displays up to 1920 by 1080 pixels. The digital flat-panel display can have pixel depths of 8, 16, or 32 for a display up to 1600 by 1024 pixels.

For information about the monitor connector and display resolutions, see “Video Monitor Ports” (page 51).

CHAPTER 3

# Input and Output Devices

This chapter describes the Power Mac G4 computer's built-in I/O devices and the ports for connecting external I/O devices. Each of the following sections describes an I/O port or device.

# USB Ports

The Power Mac G4 has two external Universal Serial Bus (USB) ports on the back. The USB ports are used for connecting the keyboard and mouse as well as additional I/O devices such as printers, scanners, and low-speed storage devices.

Each USB port is connected to a separate USB root hub, allowing both USB ports to support 12 Mbps devices at the same time with no degradation of their performance. (USB port 2 is shared internally with the USB signals to the ADC monitor.)

For more information about USB on Macintosh computers, please refer to Apple Computer's Mac OS USB DDK API Reference and the other sources listed in "USB Interface" (page 69).

## USB Connectors

The USB ports use USB Type A connectors, which have four pins each. Two of the pins are used for power and two for data. Figure 3-1 shows the connector and Table 3-1 shows the signals and pin assignments.

**Figure 3-1** USB connector

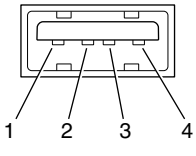


**Table 3-1** Signals on the USB connector

| Pin | Signal name | Description |
|---|---|---|
| 1 | VCC | +5 VDC |
| 2 | D– | Data – |
| 3 | D+ | Data + |
| 4 | GND | Ground |

The Power Mac G4 provides power for the USB ports at 5 V and up to 500 mA on each port. The ports share the same power supply; a short circuit on one will disable both ports until the short has been removed.

The USB ports support both low-speed and high-speed data transfers, at 1.5 Mbits per second and 12 Mbits per second, respectively. High-speed operation requires the use of shielded cables.

The Macintosh system software supports all four data transfer types defined in the USB specification.

## USB Features

Features of the USB ports include the ability to wake the computer out of Sleep mode and the ability to start up the computer from a USB mass-storage device.

“Waking Up From Sleep”

“Booting from USB Storage Devices”

### Waking Up From Sleep

USB devices can provide a remote wakeup function for the computer. The USB root hub in the computer is set to support remote wakeup whenever a device is attached to or disconnected from the bus. The device wakes the computer by sending a Resume event to the USB root hub. The mouse and keyboard that come with the computer use this method to wake the computer on a key press or mouse motion.

This functionality is part of the USB-suspend mode defined in the USB specification. Information about the operation of USB-suspend mode on Macintosh computers is included in the Mac OS USB DDK API Reference,

available on the World Wide Web at http://developer.apple.com/techpubs/hardware/DeviceManagers/usb/ usb.html

### Booting from USB Storage Devices

The Power Mac G4 can boot from a USB storage device that follows the USB Mass Storage Class specification.

Class drivers are software components that are able to communicate with many USB devices of a particular kind. If the appropriate class driver is present, any number of compliant devices can be plugged in and start working immediately without the need to install additional software. The Mac OS for the Power Mac G4computer includes USB Mass Storage Support 2.0, a class driver that supports devices that meet the USB Mass Storage Class specification.

## FireWire Ports

The Power Mac G4 includes two external FireWire (IEEE 1394) ports on the rear panel of the enclosure. The FireWire ports

- support serial I/O at 100, 200, and 400 Mbps (megabits per second)
- provide 15 watts of power when the computer system is on
- support up to 62 devices
- accept external power input on the bus when the computer is off

The FireWire hardware and software provided with the Power Mac G4 are capable of all asynchronous and isochronous transfers defined by IEEE standard 1394.

For more information about FireWire on Macintosh computers, please refer to the Apple FireWire website and the other sources listed in “FireWire Interface” (page 70).

## FireWire Connector

The FireWire connector has six contacts, as shown in Figure 3-2. The connector signals and pin assignments are shown in Table 3-2.

**Figure 3-2** FireWire connector

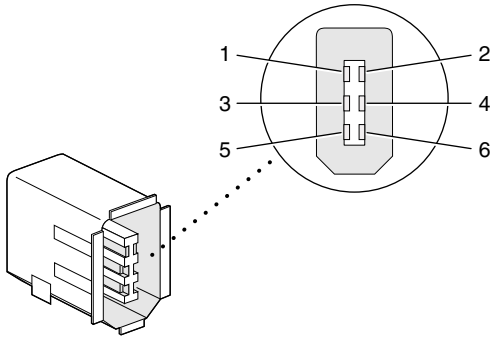



**Table 3-2** Signals on the FireWire connector

| Pin | Signal name | Description |
|---|---|---|
| 1 | Power | Unregulated DC; 30 V no load |
| 2 | Ground | Ground return for power and inner cable shield |
| 3 | TPB- | Twisted-pair B, differential signals |
| 4 | TPB+ | |
| 5 | TPA- | Twisted-pair A, differential signals |
| 6 | TPA+ | |
| Shell | — | Outer cable shield |

The power pin provides up to 15 W total power on both connectors. The voltage on the power pin is unregulated, ranging from 20 V under a typical load to 30 V under no load. The power pin also accepts external power at 8 to 33 V, in conformity with the 1394 standard, to keep the FireWire bus connected when the computer is turned off.

Pin 2 of the 6-pin FireWire connector is ground return for both power and the inner cable shield. In a FireWire cable with a 4-pin connector on the other end, such as the one included with the computer, the wire from pin 2 is connected to the shell of the 4-pin connector.

The signal pairs are crossed in the cable itself so that pins 5 and 6 at one end of the cable connect with pins 3 and 4 at the other end. When transmitting, pins 3 and 4 carry data and pins 5 and 6 carry clock; when receiving, the reverse is true.

## FireWire Device Programming

Developers of FireWire peripherals are required to provide device drivers. A driver for DV (digital video) is included in QuickTime 4.0.

### Booting from a FireWire Device

The Power Mac G4 can boot from a FireWire storage device that implements SBP-2 (Serial Bus Protocol) with the RBC (reduced block commands) command set. Detailed information is available from Developer Technical Support at dts@apple.com.

It is possible to connect two computers to each other using a FireWire cable, but no software is provided to make use of such a connection.

For additional information about the FireWire interface and the Apple APIs for FireWire device control, see the references shown in “FireWire Interface” (page 70).

### Target Disk Mode

The user has the option at boot time to put the computer into a mode of operation called Target Disk Mode (TDM). This mode is similar to SCSI Disk mode on a PowerBook computer equipped with a SCSI port, except it uses a FireWire connection instead of a special SCSI cable.

When the Power Mac G4 computer is in Target Disk Mode and connected to another Macintosh computer by a FireWire cable, the Power Mac G4 operates

like a FireWire mass storage device with the SBP-2 (Serial Bus Protocol) standard. Target Disk Mode has two primary uses:

- high-speed data transfer between computers
- diagnosis and repair of a corrupted internal hard drive

The Power Mac G4 can operate in Target Disk Mode as long as the other computer has a FireWire port and the FireWire 2.3 or newer driver.

**IMPORTANT**
For Target Disk Mode operation, only the Power Mac G4 and the host Macintosh computer can be connected to the FireWire bus. Any other FireWire devices must be disconnected. ▲

To put the Power Mac G4 computer into Target Disk mode, you restart the computer and holds down the T key until the FireWire icon appears on the display. You then connect a FireWire cable from the Power Mac G4 computer to the other computer. When the other computer completes the FireWire connection, a TDM icon appears on its display.

If you disconnect the FireWire cable or turn off the Power Mac G4 computer while in Target Disk Mode, an alert appears on the other computer asking you to reconnect the TDM volume.

To take the Power Mac G4 computer out of Target Disk Mode, you drag the TDM icon on the other computer to the trash, then press the power button on the Power Mac G4.

For more information about Target Disk Mode, see the section "Target Mode" in Technote 1189, *The Monster Disk Driver Technote*.

# Ethernet Port

The Power Mac G4 has a built-in Ethernet port that supports 10Base-T, 100Base-T, and 1000Base-T transfer rates. In operation, the actual speed of the link is auto-negotiated between the computer's PHY device and the network bridge or router to which it is connected.

The connector for the Ethernet port is an RJ-45 connector on the back of the computer. Table 3-3 shows the signals and pin assignments for 10Base-T and 100Base-T operation. Table 3-4 shows the signals and pin assignments for 1000Base-T operation.

**Table 3-3** Signals for 10Base-T and 100Base-T operation

| Pin | Signal name | Signal definition |
|---|---|---|
| 1 | TXP | Transmit (positive lead) |
| 2 | TXN | Transmit (negative lead) |
| 3 | RXP | Receive (positive lead) |
| 4 | – | Not used |
| 5 | – | Not used |
| 6 | RXN | Receive (negative lead) |
| 7 | – | Not used |
| 8 | – | Not used |

**Table 3-4** Signals for 1000Base-T operation

| Pin | Signal name | Signal definition |
|---|---|---|
| 1 | TRD+(0) | Transmit and receive data 0 (positive lead) |
| 2 | TRD–(0) | Transmit and receive data 0 (negative lead) |
| 3 | TRD+(1) | Transmit and receive data 1 (positive lead) |
| 4 | TRD+(2) | Transmit and receive data 2 (positive lead) |
| 5 | TRD–(2) | Transmit and receive data 2 (negative lead) |
| 6 | TRD–(1) | Transmit and receive data 1 (negative lead) |
| 7 | TRD+(3) | Transmit and receive data 3 (positive lead) |
| 8 | TRD–(3) | Transmit and receive data 3 (negative lead) |

To interconnect two computers for 1000Base-T operation, you must use 4-pair cable (Category 5 or 6).

The Ethernet interface in the Power Mac G4 conforms to the ISO/IEC 802.3 specification, where applicable, and complies with IEEE specifications 802.3i (10Base-T), 802.3u-1995 (100Base-T), and 802.3ab (1000Base-T).

# Disk Drives

The Power Mac G4 has an Ultra DMA/66 (ATA-5) interface and an ATA-3 interface for internal mass storage and removable media devices. The enclosure includes data and power connectors for the boot drive and a second internal drive on the Ultra DMA/66 interface. It also has a power connector for a third internal drive. The enclosure has data and power connectors for the internal ATAPI DVD-ROM or DVD-RAM drive and an internal ATAPI Zip drive. Those drives are connected to the ATA-3 interface.

The enclosure includes three drive bays for mass storage devices. One bay is occupied by the boot drive. A drive in one of the other bays can be connected to the second drive connector on the Ultra DMA/66 cable assembly or to an optional or user installed third-party PCI controller card. None of the drive bays can be modified to support removable drive bay kits.

The Ultra DMA/66 bus supports PIO Mode 4, DMA Mode 2, and Ultra DMA Mode 2 data transfers. The ATA-3 bus supports PIO Mode 4 and DMA Mode 2 data transfers.

The ATA-3 channel supports two ATA devices. The devices are configured in a ATA Device 0/1 configuration. The ATAPI DVD-ROM and Zip drive, when installed, occupy both device locations on the ATA-3 channel. The ATAPI DVD-ROM is Device 0 (master), and the Zip drive is Device 1 (slave). If the Zip drive is not factory installed in the system, a power and data cable is available for adding a Zip drive to the ATA-3 bus in the Zip drive bay. The device must be device-select jumpered as Device 1 (slave).

## Ultra DMA/66 Hard Disk

The logic board supports an internal hard disk that uses the standard Ultra DMA/66 (ATA-5) interface. The computer comes with an Ultra DMA/66 hard disk or a Wide Ultra 2 hard disk installed in the third drive bay.

The internal hard disk has a 40-pin connector and a separate 4-pin power connector. An 80-conductor high-density cable with a 40-pin connector is attached to the main logic board. To provide improved signal quality, the 80-conductor cable has ground lines separating the signals on the 40-pin connector. The power cable is attached directly to the power supply.

## DVD-ROM Drive

The Power Mac G4 has an internal 8x-speed DVD-ROM drive. It supports the following disc formats:

- DVD-RAM: bare one- or two sided disc, reading only
- DVD-ROM: one- or two-layer, one- or two-sided
- CD-ROM (Modes 1 and 2), CD-ROM XA (Mode 2, Forms 1 and 2)
- CD-Audio, Photo CD, CD-RW, CD-R, CD-Extra
- CD-I (Mode 2, Forms 1 and 2), CD-I Ready, CD-I Bridge
- Video CD

The DVD-ROM drive is an ATAPI drive and is connected as device 0 in an ATA Device 0/1 configuration on the ATA-3 channel of the main logic board. To provide improved signal quality, the ATA bus has an 80-conductor cable with ground lines separating the signals.

## DVD-RAM Drive

Some configurations of the Power Mac G4 have an internal 2x-speed DVD-RAM drive in place of the DVD-ROM drive. The DVD-RAM drive reads DVD-ROM at 6x speed.

The DVD-RAM drive supports the following disc formats.

- Reading and writing:
  - DVD-RAM media in Type 1 cartridge, one- or two-sided
  - DVD-RAM media in Type 2 cartridge, one sided
- Reading only:
  - DVD-RAM bare one-sided disc, reading only
  - DVD-R (3.9 GB, disc-at-once only)

- DVD-ROM (One- or two-layer, one- or two-sided)
- CD-ROM (Modes 1 and 2)
- CD-ROM XA (Mode 2, Forms 1 and 2)
- CD-Audio (CD-DA data through IDE bus)
- Photo CD (single and multiple sessions)
- CD-RW
- CD-R (fixed and variable packets)
- CD-I (Mode 2, Forms 1 and 2), CD-I Ready, CD-I Bridge
- Video CD (White Book disc)
- CD-EXTRA CD (Blue Book disc)

The DVD-RAM drive takes the place of the DVD-ROM drive and is connected in the same way: as device 0 in an ATA Device 0/1 configuration on the ATA-3 channel of the main logic board. To provide improved signal quality, the ATA bus has an 80-conductor cable with ground lines separating the signals.

## Optional Zip Drive

As an option, the Power Mac G4 can have an internal Iomega Zip drive. It is an ATAPI drive connected as device 1 in an ATA Device 0/1 configuration on the EIDE channel of the main logic board. If the Zip drive option is not installed at the time of purchase, data and power connectors are provided to add an ATAPI Zip drive to the system. The device should be device-select jumpered as device 1 (slave).

## Optional Ultra SCSI 160 Drive

An Ultra SCSI 160 drive and Ultra SCSI 160 PCI controller card are available as a configuration option. The Ultra SCSI 160 is a low-voltage differential (LVD) interface and provides data transfer rates of up to 160 MB per second. For additional information about Ultra SCSI, refer to the reference shown in “Ultra SCSI Interface” (page 69).

# Internal Modem

The Power Mac G4 has a dedicated slot for an internal modem module. The module is available as a build-to-order option or as a user-installable upgrade. The external I/O connector for the modem is an RJ-11 connector installed on the rear of the computer. The modem has the following features:

- modem bit rates up to 56 Kbps (supports K56flex and V.90 modem standards)
- fax modem bit rates up to 14.4 Kbps

The modem appears to the system as a serial port that responds to the typical AT commands. The modem provides a sound output for monitoring the progress of the modem connection.

**Note**
This developer note does not provide electrical or mechanical specifications for the modem slot.

# AirPort Card Wireless LAN Module

The Power Mac G4 supports the AirPort Card, an internal wireless LAN module. The AirPort Card is available as a build-to-order option or as a user-installable upgrade.

The AirPort Card can be used for local printer sharing, file exchange, internet access, and e-mail access.

The AirPort Card transmits and receives data at up to 11 Mbps. It is also interoperable with some older wireless LANs, as specified in “Hardware Components” (page 45).

Wireless connection to the internet or a wired LAN requires a base station as the connection to the internet or a bridge between the wireless signals and a wired LAN. Software included with the AirPort Card enables a Macintosh computer that has an AirPort Card installed to act as a base station. The user also has the

option of purchasing an AirPort Base Station that can be connected to the wired LAN or to a 56 Kbps hardware modem.

## Data Security

Three features of the AirPort Card help to maintain the security of data transmissions:

- The system uses direct-sequence spread-spectrum (DSSS) technology that uses a multi-bit spreading code that effectively scrambles the data for any receiver that lacks the corresponding code.
- The system can use a table of authentic network client ID values to verify each client's identity before granting access to the network.
- When communicating with a base station, the system encrypts the data using Wired Equivalent Privacy (WEP) with a 40-bit security key.

## Hardware Components

The AirPort Card is a wireless LAN module based on the IEEE 802.11 standard and using direct-sequence spread-spectrum (DSSS) technology. It is interoperable with PC-compatible wireless LANs that conform to the 802.11 standard and use DSSS.

The AirPort Card contains a media access controller (MAC), a digital signal processor (DSP), and a radio-frequency (RF) section. The antennas are built into the computer's case.

The MAC provides the data communication protocols and the controls for the physical layer.

The DSP provides the core physical layer functionality and controls the RF section. The DSP communicates with the MAC for data exchange, physical layer control, and parameter settings.

The RF section provides modulation and transmission of outgoing signals and reception and demodulation of incoming signals. Its power output when transmitting is nominally 31 mW.

When transmitting data, the DSP converts the outgoing data stream into a DSSS signal and sends it to the RF section. When receiving data, the DSP accepts incoming DSSS data from the RF section and converts it to a normal data stream.

Two antennas are connected to the AirPort Card. One antenna is always used for transmitting. Either of the two antennas may be used for receiving. Using a diversity technique, the DSP selects the antenna that gives the best reception.

### Software Components

Software that is provided with the AirPort Card includes

- AirPort Setup Assistant, a standalone assistant that takes users through the steps necessary to set up the AirPort Card, set up an AirPort Base Station, or set up a software base station.
- AirPort Application, an application that allows users to switch between wireless networks and to create and join peer-to-peer networks.
- AirPort Control Strip module, which provides a signal strength indication and most of the functions of the AirPort Application.
- AirPort Utility, a utility for the advanced user. With it the user can edit the administrative and advanced settings for a hardware or software base station. It can also be used to determine the location for the base station that gives the best reception.

## Keyboard

The Power Mac G4 comes with a Apple Pro Keyboard. It is a full-size keyboard with function keys and separate keypad and editing sections.

The keyboard has an attached 1-meter cable and comes with a 1-meter extender cable for installations where the computer is located on the floor or away from the immediate desktop area.

### Keyboard Features

Here is a list of the features of the Apple Pro Keyboard.

- Slope settable to either 0 or 6 degrees
- 108 keys (on the ANSI versions)
- 15 function keys, programmable by the user

- 6 editing keys (Page Up, Page Down, Home, End, Forward Delete, and Help)
- USB HID Consumer Page Usage control keys (Volume Up, Volume Down, Mute, and Eject)
- Full travel, standard pitch keys on alphanumeric, editing, and keypad sections, including function keys and cursor position keys
- Localized worldwide: 33 versions, 3 standard layouts (ANSI, JIS, ISO)
- LED indicators in the Caps Lock and Num Lock keys
- USB hub functionality with two USB sockets

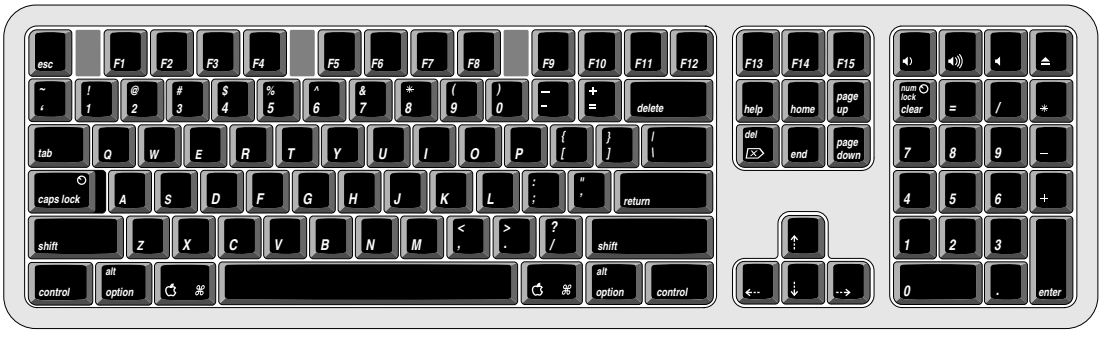
**Note**
There is no power key on this keyboard. ◆

## Keyboard Layout

There are localized versions of the Apple Pro Keyboard for use in different parts of the world. The three standards used are ANSI (US and North America), JIS (Japan), and ISO (Europe). Figure 3-3 shows the keyboard layout for the ANSI keyboard. Applications can determine which keyboard is connected by calling the Gestalt Manager and checking for the corresponding value of the `gestaltKeyboardType` selector:

- `gestaltUSBAndyANSIKbd` (value = 204)
- `gestaltUSBAndyISOKbd` (value = 205)
- `gestaltUSBAndyJISKbd` (value = 206)

**Figure 3-3** ANSI keyboard layout




## Programming the Function Keys

The function keys (F1–F15) can be programmed by the user through the Keyboard Control Panel. Operations that can be assigned include

- opening an application
- opening a document
- evoking an AppleScript
- logging on to a file server by way of an alias

## Multi-Media Control Keys

The keyboard has four multi-media keys: Volume Up, Volume Down, Mute, and Eject. The provide direct control of the those features on the computer by way of the USB.

## Keyboard and USB

The Apple Pro Keyboard is designed to work with the computer by way of the USB ports. The keyboard has a captive cable with a USB Type A connector. The keyboard is a bus-powered USB hub with two USB Type A ports.

▲ **WARNING**
A bus-powered hub as defined in the USB specification does not provide enough power to support a second bus-powered hub. A second bus-powered hub must be connected to the second USB port on the computer, not to a port on the keyboard. ▲

The NMI and reset key combinations now use the Eject key. The keys are decoded in software and may not be available under some crashed conditions. Therefore, NMI and reset switches are also available on the front of the computer.

Apple provides a HID class driver for the Apple Pro Keyboard, which supports the USB boot protocol. Other keyboards intended for use on the Macintosh platform must support the HID boot protocol, as defined in the USB Device Class Definition for Human Interface Devices (HIDs). p

# Mouse

The iMac comes with an Apple Pro Mouse. The mouse case is made of polycarbonate plastic like the computer.

The Apple Pro Mouse is a new design that uses optical tracking in place of the traditional rolling ball. It works on almost any surface, though non-reflective, opaque surface without repetitive patterns work best.

# Sound System

The sound system for the Power Mac G4 supports 44.1 kHz 16-bit stereo sound output and input, available simultaneously.

Like other Macintosh computers, the sound circuitry and system software can create sounds digitally and either play the sounds through speaker inside the enclosure or send the sound signals out through the sound output jack. The computer also records sound data from several sources: a PlainTalk microphone, a stereo sound source connected to the line-level sound input jack, or single-channel sound signals from the modem card in the internal modem

slot. With each sound input source, sound playthrough can be enabled or disabled.

In addition to the signal sources connected to the sound system, the computer also accepts digital sound data from the DVD drive and from devices connected to the USB and FireWire ports. Sound data from those sources can be sent to the sound system to be converted to analog form for output to the speakers and the output jack.

## Sound Output Jack

The Power Mac G4 has one built-in speaker and a 3.5 mm mini jack for stereo sound output on the back of the enclosure.

The output jack is suitable for connecting a pair of headphones or amplified external speakers. Inserting a plug into the sound output jack disconnects the internal speaker.

The sound output jack has the following electrical characteristics:

- output sound signal-to-noise ratio (SNR) <90 dB unweighted (typical) when sound playback is from system hard disk drive or main memory
- output sound SNR <80 dB unweighted (nominal) when playback is from CD
- overall output sound SNR <90 dB unweighted (typical)

## Sound Input Jack

The Power Mac G4 has a stereo sound input jack on the back of the enclosure for connecting an external PlainTalk microphone or a line-level sound source. The sound input jack accepts a standard 3.5 mm stereophonic phone plug (two signals plus ground).

The sound input jack has the following electrical characteristics:

- input impedance: 20 kΩ
- maximum input level without distortion: 2.5 V peak to peak (Vpp) maximum
- line-level microphone voltage range of 0.28 V to 2.1 V peak to peak
- input SNR <90 dB unweighted (typical) for recording to system hard disk drive or system main memory

### Digitizing Sound

The sound circuitry digitizes and records sound as 44.1 kHz 16-bit samples. If a sound sampled at a lower rate on another computer is played as output, the Sound Manager transparently upsamples the sound to 44.1 kHz prior to outputting the audio to the Screamer sound IC.

When recording sound from a microphone, applications that are concerned about feedback should disable sound playthrough by calling the Sound Manager APIs.

## Video Monitor Ports

The Power Mac G4 comes with an accelerated graphics card installed. The card provides an Apple display connector (ADC) for a digital flat-panel monitor and a VGA connector for an analog video monitor.

### Digital Monitor Connector

The connector for the digital video monitor is an Apple proprietary connector called the ADC (Apple display connector). It carries both digital and analog video signals as well as USB and control signals and power for an external monitor. Figure 3-4 shows the contact configuration; Table 3-5 and Table 3-6 list the signals and pin assignments.

The maximum current available from the 28-V supply for the external monitor is 4.0 A.

**Figure 3-4** Apple display connector

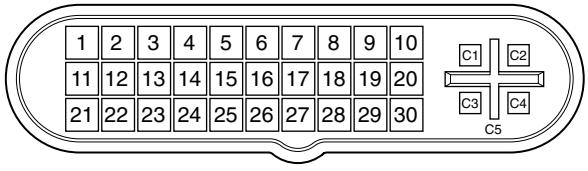



**Table 3-5** Digital signals on the Apple display connector

| Pin | Signal name | Pin | Signal name |
|---|---|---|---|
| 1 | 28-V Supply | 16 | TMDS Data1/3 Shield |
| 2 | 28-V Supply | 17 | TMDS Data3– |
| 3 | LED | 18 | TMDS Data3+ |
| 4 | TMDS Data0– | 19 | DDC CLock |
| 5 | TMDS Data0+ | 20 | Clock Return |
| 6 | TMDS Data0/5 Shield | 21 | USB Data+ |
| 7 | TMDS Data5– | 22 | USB Data– |
| 8 | TMDS Data5+ | 23 | USB Return |
| 9 | DDC Data | 24 | TMDS Data2– |
| 10 | Vsync | 25 | TMDS Data2+ |
| 11 | 28-V Return | 26 | TMDS Data2/4 Shield |
| 12 | 28-V Return | 27 | TMDS Data4– |
| 13 | Soft Power | 28 | TMDS Data4+ |
| 14 | TMDS Data1– | 29 | Clock+ |
| 15 | TMDS Data1+ | 30 | Clock– |

**Table 3-6** Analog signals on the Apple display connector

| Pin | Signal name |
|---|---|
| C1 | Analog Blue Video |
| C2 | Analog Green Video |
| C3 | Analog Horizontal Sync |
| C4 | Analog Red Video |
| C5 | Analog RGB Return and DDC Return |

The graphics data sent to the digital monitor use transition minimized differential signaling (TMDS). TMDS uses an encoding algorithm to convert bytes of graphics data into characters that are transition-minimized to reduce EMI with copper cables and DC-balanced for transmission over fiber optic cables. The TMDS algorithm also provides robust clock recovery for greater skew tolerance with longer cables or low cost short cables. For additional information about TMDS, see the references shown in “Digital Visual Interface” (page 70).

## Digital Display Resolutions

Table 3-7 shows the resolutions supported on flat-panel (digital) displays. The 16 MB of video RAM on the accelerated graphics card supports pixel depths up to 32 bits per pixel at all resolutions.

**Table 3-7** Digital display resolutions

| | |
|---|---|
| 640 by 480 | 1024 by 768 |
| 800 by 500 | 1280 by 800 |
| 800 by 512 | 1280 by 1024 |
| 800 by 600 | 1600 by 1024 |
| 1024 by 640 | 1600 by 1200 |

## Analog Monitor Connector

The connector for the video monitor is a three-row DB-9/15 (also called mini sub D15) connector for use with a VGA, SVGA, or XGA monitor. Figure 3-5 shows the pin configuration and Table 3-8 lists the signals and pin assignments.

**Figure 3-5** Analog monitor connector

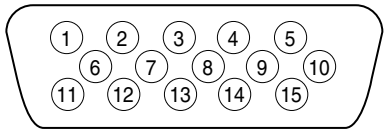



**Table 3-8** Signals on the analog monitor connector

| Pin | Signal name | Description |
|---|---|---|
| 1 | RED | Red video signal |
| 2 | GREEN | Green video signal |
| 3 | BLUE | Blue video signal |
| 4 | MONID(0) | Monitor ID signal 0 |
| 5 | GND | DDC return |
| 6 | RED_RTN | Red video signal return |
| 7 | GREEN_RTN | Green video signal return |
| 8 | BLUE_RTN | Blue video signal return |
| 9 | n.c. | No connect |
| 10 | GND | Ground |
| 11 | n.c. | No connect |
| 12 | SDA | $I^2C$ data |
| 13 | HSYNC | Horizontal synchronization signal |
| 14 | VSYNC | Vertical synchronization signal |
| 15 | SCL | $I^2C$ clock |

## Monitor Adapter

A monitor adapter is required for connecting an older Apple monitor cable to the the analog (VGA) connector. The adapter enables the computer to recognize a wide range of monitor types. The adapter does not come with the computer. The Apple part number for the adapter is 590-1120.

## Analog Display Resolutions

Table 3-9 shows the display resolutions, vertical scan rates, and maximum pixel depths supported on analog (CRT) monitors. When power is applied, the monitor is initially set for a display size of 640 by 480 pixels. With a multisync monitor the user can switch the monitor resolution during operation by using the Monitors control panel or the BitDepth and Resolution modules in the control strip.

**Table 3-9** Analog display resolutions

| Display resolution | Vertical scan rate | Pixel depth | Display resolution | Vertical scan rate | Pixel depth |
|---|---|---|---|---|---|
| 640 by 480 | 60 Hz | 32 | 1024 by 768 (VESA) | 75 Hz | 32 |
| 640 by 480 | 67 Hz | 32 | 1024 by 768 (19″ RGB) | 75 Hz | 32 |
| 640 by 480 | 72 Hz | 32 | 1024 by 768 | 85 Hz | 32 |
| 640 by 480 | 75 Hz | 32 | 1024 by 768 | 90 Hz | 32 |
| 640 by 480 | 85 Hz | 32 | 1024 by 768 | 100 Hz | 32 |
| 640 by 480 | 90 Hz | 32 | 1024 by 768 | 120 Hz | 32 |
| 640 by 480 | 100 Hz | 32 | 1152 by 870 | 75 Hz | 32 |
| 640 by 480 | 120 Hz | 32 | 1280 by 960 | 75 Hz | 32 |
| 640 by 870 | 75 Hz | 32 | 1280 by 1024 | 60 Hz | 32 |
| 800 by 600 | 56 Hz | 32 | 1280 by 1024 | 75 Hz | 32 |
| 800 by 600 | 60 Hz | 32 | 1280 by 1024 | 80 Hz | 32 |
| 800 by 600 | 72 Hz | 32 | 1600 by 1200 | 60 Hz | 32 |

**Table 3-9** Analog display resolutions (continued)

| Display resolution | Vertical scan rate | Pixel depth | Display resolution | Vertical scan rate | Pixel depth |
|---|---|---|---|---|---|
| 800 by 600 | 75 Hz | 32 | 1600 by 1200 | 65 Hz | 32 |
| 800 by 600 | 85 Hz | 32 | 1600 by 1200 | 70 Hz | 32 |
| 800 by 600 | 90 Hz | 32 | 1600 by 1200 | 75 Hz | 32 |
| 800 by 600 | 100 Hz | 32 | 1600 by 1200 | 85 Hz | 32 |
| 800 by 600 | 120 Hz | 32 | 1920 by 1080 | 60 Hz | 32 |
| 832 by 624 | 75 Hz | 32 | 1920 by 1080 | 72 Hz | 32 |
| 1024 by 768 | 60 Hz | 32 | 1920 by 1200 | 76 | 32 |
| 1024 by 768 | 70 Hz | 32 | | | |

CHAPTER 4

# Expansion

This chapter describes the expansion features of the Power Mac G4 computer: the RAM expansion slot and the PCI expansion slots.

# RAM Expansion

The main logic board has four RAM expansion slots for SDRAM DIMMs. At least one of the RAM expansion slots contains a factory installed SDRAM DIMM.

The SDRAM DIMMs can be installed one or more at a time. The system supports linear memory organization; no performance gains are seen when two DIMMs of the same size are installed. Any supported size DIMM can be installed in any DIMM slot, and the combined memory of all of the DIMMs installed is configured as a contiguous array of memory.

The maximum memory size supported by Mac OS 9 is 1.5 GB.

## DIMM Specifications

The RAM expansion slots accept 168-pin SDRAM DIMMs that are 3.3 volt, unbuffered, 8-byte, nonparity, and PC100 compliant. The speed of the SDRAM devices must be rated at 125 MHz (8 ns) or faster.

The DIMMs can be implemented with either SDRAM or ESDRAM devices. ESDRAM devices provide higher performance for random read and write operations, but SDRAM devices are generally available in larger sizes.

**IMPORTANT**
DIMMs with any of the following features are not supported in the Power Mac G4: registers or buffers, PLLs, ECC, parity, or EDO RAM. ▲

### Mechanical Specifications

The mechanical design of the SDRAM DIMM is defined by the JEDEC MO-161-D specification. To find this specification on the World Wide Web, refer to “RAM Expansion Modules” (page 68).

The maximum height of DIMMs for use in the Power Mac G4 computer is 2.00 inches.

### Electrical Specifications

The electrical design of the SDRAM DIMM is defined by the JEDEC standard 21-C specification. To find this specification on the World Wide Web, refer to "RAM Expansion Modules" (page 68).

The presence detect serial EEPROM specified in the JEDEC standard is required and must be set to properly define the DIMM configuration. Details about the required values for each byte on presence detect EEPROM can be found in sections 4.5.4 and 4.1.2.5 of the JEDEC standard 21-C specification.

Capacitance of the data lines must be kept to a minimum. Individual DRAM devices should have a pin capacitance of not more than 5 pF on each data pin.

**IMPORTANT**

RAM modules for the Power Mac G4 must conform to the PC100 specification. In particular, they must behave correctly when the CKE signal is low, as defined in the specification. ▲

## DIMM Configurations

The largest DIMM supported is a two-bank DIMM of 512 MB using 256 Mbit SDRAM devices. The minimum bank size supported by the memory controller is 2 MB, and the largest is 256 MB. The maximum number of devices per DIMM is 16.

**Note**

With four DIMMs of 512 MB each, the Power Mac G4 can accommodate 2 GB of memory. At present, the Mac OS supports up to 1.5 GB of memory, with a 999 MB maximum for each application. ◆

Table 4-1 shows information about the different sizes of SDRAM devices used in the memory modules. The memory controller supports 64 Mbit, 128 Mbit, and 256 Mbit SDRAM devices. The device configurations include three specifications: address range, word size, and number of banks. For example, a 1 M by 16 by 4 device addresses 1 M, stores 16 bits at a time, and has 4 banks.

The third column in Table 4-1 specifies the number of devices needed to make up the 8-byte width of the data bus. The fourth column in the table shows the size of each bank of devices, which is based on the number of internal banks in each device and the number of devices per bank. The last column shows the memory size of the largest DIMM with that device size that the computer can accommodate.

**Table 4-1** Sizes of RAM expansion devices and DIMMs

| SDRAM device size | Device configuration | Devices per bank | Size of each bank | Size of DIMM |
|---|---|---|---|---|
| 64 Mbits | 4 M x 8 x 2 | 8 | 64 MB | 128 MB |
| 64 Mbits | 2 M x 8 x 4 | 8 | 64 MB | 128 MB |
| 64 Mbits | 2 M x 16 x 2 | 4 | 32 MB | 64 MB |
| 64 Mbits | 1 M x 16 x 4 | 4 | 32 MB | 64 MB |
| 64 Mbits | 1 M x 32 x 2 | 2 | 16 MB | 32 MB |
| 64 Mbits | 512 K x 32 x 4 | 2 | 16 MB | 32 MB |
| 128 Mbits | 4 M x 8 x 4 | 8 | 128 MB | 256 MB |
| 128 Mbits | 2 M x 16 x 4 | 4 | 64 MB | 128 MB |
| 128 Mbits | 1 M x 32 x 4 | 2 | 32 MB | 64 MB |
| 256 Mbits | 8 M x 8 x 4 | 8 | 256 MB | 512 MB |
| 256 Mbits | 4 M x 16 x 4 | 4 | 128 MB | 256 MB |
| 256 Mbits | 2 M x 32 x 4 | 2 | 64 MB | 128 MB |

## RAM Addressing

Signals A[0–12] on each SDRAM DIMM make up a 13-bit multiplexed address bus that can support several different sizes of SDRAM devices. Table 4-2 shows the address multiplexing modes used with the devices.

**Table 4-2** Address multiplexing modes for SDRAM devices

| Device size | Device configuration | Size of row address | Size of column address |
|---|---|---|---|
| 64 Mbits | 4 M x 8 x 2 | 13 | 9 |
| 64 Mbits | 2 M x 8 x 4 | 12 | 9 |
| 64 Mbits | 2 M x 16 x 2 | 13 | 8 |
| 64 Mbits | 2 M x 16 x 2 | 11 | 10 |
| 64 Mbits | 1 M x 16 x 4 | 12 | 8 |
| 64 Mbits | 1 M x 32 x 2 | 11 | 9 |
| 64 Mbits | 512 K x 32 x 4 | 11 | 8 |
| 128 Mbits | 4 M x 8 x 4 | 12 | 10 |
| 128 Mbits | 2 M x 16 x 4 | 12 | 9 |
| 128 Mbits | 1 M x 32 x 4 | 12 | 8 |
| 256 Mbits | 8 M x 8 x 4 | 13 | 10 |
| 256 Mbits | 4 M x 16 x 4 | 13 | 9 |
| 256 Mbits | 2 M x 32 x 4 | 13 | 8 |

# PCI Expansion Slots

The main logic board uses the industry-standard peripheral component interconnect (PCI) bus for an I/O expansion bus. It is a 33 MHz bus with 64-bit multiplexed address and data.

The Power Mac G4 also has an AGP graphics slot, which is labeled 1. It accommodates standard 32-bit, 66 MHz AGP-2X cards. The computer is always configured with a graphics card installed in slot 1, so that slot is not available for PCI card expansion. For information about the graphics card, see "AGP Graphics Card" (page 29).

Expansion slots 2, 3, and 4 accommodate 33 MHz PCI cards with either 32-bit or 64-bit address and data buses. The PCI cards can use power at +5 V, +3.3 V, or both. The slots accept standard 6.88-inch and 12.283-inch PCI cards as defined by the *PCI Local Bus Specification*, Revision 2.1. The cards are required to use the standard ISA fence described in the specification.

The expansion slots support all the required PCI signals and certain optional PCI signals. The PCI slots support the optional 64-bit bus extension signals and cache support signals.

The PCI slots and the AGP slot carry the 3.3V_AUX power and PME signals to allow an expansion card to wake the computer from Sleep mode.

The maximum power available on the AGP slot is 8 watts. The maximum total power available for all three PCI slots is 45 watts.

To install or remove a PCI card, the user first opens the door of the enclosure. Then the user removes the blank PCI fence for the appropriate slot, inserts the card in the slot, and screws the card's fence into place to secure the card. The user then closes the enclosure door and turns on the computer. In order to use the new PCI card, a driver must be installed. The driver installation procedure is documented by the manufacturer of the PCI card in question.

**IMPORTANT**

The user should first shut down the computer before removing or installing PCI cards. The Power Mac G4 does not support PCI hot-plugging functionality. The main logic board has a red light to let the user know that power is present. ▲

For more information about the PCI expansion slot, refer to *Designing PCI Cards and Drivers for Power Macintosh Computers.*

APPENDIX A

# Supplemental Reference Documents

For more information about the technologies mentioned in this developer note, you may wish to consult some of the references listed in the following sections.

For information about older models of Macintosh computers, refer to the developer notes archive at

http://developer.apple.com/techpubs/hardware/hardware2.html

You should also have copies of the relevant books describing the system software for Macintosh computers available in technical bookstores and on the World Wide Web at

http://developer.apple.com/techpubs/mac/mac.html

## PowerPC G4 Microprocessor

Information about the PowerPC™ G4 microprocessor is available on the World Wide Web at

http://www.mot.com/SPS/PowerPC/index.html

## Velocity Engine (AltiVec)

Velocity Engine is Apple's name for the AltiVec vector processor in the PowerPC G4 microprocessor. Apple provides support for developers who are starting to use the Velocity Engine in their applications. Documentation, development tools, and sample code are now available on the World Wide Web, at

http://developer.apple.com/hardware/altivec/index.html

*AltiVec Technology Programming Environments Manual* (AltiVec PEM) is a reference guide for programmers. It contains a description for each instruction and information to help in understanding how the instruction works. You can

obtain a copy of the AltiVec PEM through the Motorola AltiVec site on the World Wide Web, at

http://www.mot.com/SPS/PowerPC/AltiVec/facts.html

## Multiprocessing Services

The Multiprocessing Services API allows your application to create tasks that run independently on one or more processors. The Multiprocessing 2.1 SDK includes interfaces and libraries, documentation, demonstration applications, and sample code. You can download the SDK from Apple's developer site on the World Wide Web at

ftp://ftp.apple.com/developer/Development_Kits/Multiprocessing_2.0_SDK.sit.hqx

## 3D Graphics

Developers of 3D graphics for games should know about OpenGL for Macintosh, a new version of SGI's application programming interface (API) and software library for 3D graphics.

Information is available on the World Wide Web at

http://www.apple.com/opengl

Developer support and documentation is available at

http://developer.apple.com/opengl/

If you are interested in taking advantage of the 3D graphics acceleration features available on the graphics card, you should have *3D Graphics Programming With QuickDraw 3D.* The current documentation for QuickDraw 3D is part of the QuickTime documentation and is available on the World Wide Web at

http://developer.apple.com/techpubs/quicktime/qtdevdocs/QD3D/qd3d_book.htm

# Mac OS 9

For a description of the version of the Mac OS that comes with the new models, you should refer to the technote for Mac OS 9. Other technotes contain information about the NewWorld software architecture and the API changes for Power Manager 2.0. The technotes are available on the Technote website at

http://developer.apple.com/technotes/

You should also have copies of the relevant books describing the system software for Macintosh computers available in technical bookstores and on the World Wide Web at

http://developer.apple.com/techpubs/mac/mac.html

# ROM-in-RAM Architecture

The system software in all current Macintosh computers uses a ROM-in-RAM approach, also called the New World architecture. For more information about this architecture, see Technote 1167, *NewWorld Architecture,* available on Apple's technote website at

http://developer.apple.com/technotes/tn/tn1167.html

With the ROM-in-RAM approach, memory is not mapped one-to-one as it was for earlier PCI-based Macintosh computers. This could be a compatibility issue with some software. For more information see Technical Q&A DV 33, *PrepareMemoryForIO for the New World*, available on Apple's technote website at

http://developer.apple.com/qa/dv/dv33.html

# Open Firmware

The ROM-in-RAM software architecture implemented on the Power Mac G4 computer follows some of the standards defined by the Open Firmware IEEE 1274-1994 specification. Three Technotes provide an introduction to Open Firmware on the Macintosh platform. They are:

*TN 1061: Open Firmware, Part I*, available on the Technote web site at

http://developer.apple.com/technotes/tn/tn1061.html

*TN 1062: Open Firmware, Part II*, available on the Technote web site at

http://developer.apple.com/technotes/tn/tn1062.html

*TN 1044: Open Firmware, Part III*, available on the Technote web site at

http://developer.apple.com/technotes/tn/tn1044.html

# RAM Expansion Modules

The Power Mac G4 computer uses PC100 compliant, 168-pin SDRAM DIMMs. The mechanical characteristics of the DIMM are given in the JEDEC specification for the 168-pin 8-byte DRAM DIMM. The specification number is JEDEC MO-161; the specification is available from the Electronics Industry Association's website at

http://www.jedec.org/download/pub95/

The electrical characteristics of the DIMM are given in section 4.5.6 of the JEDEC Standard 21-C, release 7. The specification is available from the Electronics Industry Association's website at

http://www.jedec.org/download/pub21/

The RAM DIMMs are required to be PC100 compliant. The PC100 specification is available from Intel's website at

http://developer.intel.com/design/chipsets/memory/sdram.htm#S1

# ATA Devices

ATA Manager 4.0 supports driver software for internal IDE drives and includes DMA support. For the latest information about ATA Manager 4.0, see *Technote #1098, ATA Device Software Guide Additions and Corrections,* available on the world wide web at

http://developer.apple.com/technotes/tn/tn1098.html

The web page for Technote #1098 includes a link to a downloadable copy of *ATA Device Software Guide*.

# Ultra SCSI Interface

Ultra SCSI disk drives and Ultra SCSI PCI controller cards are available as configuration options on some Macintosh models. Information about the Ultra SCSI interface can be found at

http://www.quantum.com/src/whitepapers/

# USB Interface

For more information about USB on the Macintosh computer, refer to Apple Computer's *Mac OS USB DDK API Reference.* Information is also available on the World Wide Web, at:

http://developer.apple.com/techpubs/hardware/DeviceManagers/usb/usb.html

USB game controllers are supported by the InputSprocket component of the Apple Games Sprockets software architecture. InputSprocket software and information about the InputSprocket APIs can be found at

http://developer.apple.com/games/

For full specifications of the Universal Serial Bus, you should refer to the USB Implementation Forum on the World Wide Web, at:

http://www.usb.org/developers/index.html

# FireWire Interface

For additional information about the FireWire IEEE 1394a interface and the Apple APIs for FireWire software, refer to the resources available on the Apple FireWire website at

http://developer.apple.com/hardware/FireWire/index.html

The IEEE 1394a draft standard is available from the IEEE; you can order that document electronically from the IEEE Standards Department website at

http://standards.ieee.org/catalog/bus.html

You may also find useful information at the 1394 trade association's website at

http://www.1394ta.org/

# Digital Visual Interface

For information about transition minimized differential signaling (TMDS) used with digital video monitors, see the specification, *Digital Visual Interface DVI Revision 1.0*, available on the web site of the Digital Display Working Group (DDWG) at

http://www.ddwg.org/index.html

APPENDIX B

# Conventions and Abbreviations

This developer note uses the following typographical conventions and abbreviations.

## Typographical Conventions

**Note**
A note like this contains information that is of interest but is not essential for an understanding of the text. ◆

**IMPORTANT**
A note like this contains important information that you should read before proceeding. ▲

## Abbreviations

When unusual abbreviations appear in this developer note, the corresponding terms are also spelled out. Standard units of measure and other widely used abbreviations are not spelled out.

Here are the standard units of measure used in developer notes:

| | | | |
|---|---|---|---|
| A | amperes | mA | milliamperes |
| dB | decibels | µA | microamperes |
| GB | gigabytes | MB | megabytes |
| Hz | hertz | MHz | megahertz |
| in. | inches | mm | millimeters |
| k | 1000 | ms | milliseconds |
| K | 1024 | µs | microseconds |

| | | | |
|---|---|---|---|
| KB | kilobytes | ns | nanoseconds |
| kg | kilograms | Ω | ohms |
| kHz | kilohertz | sec. | seconds |
| kΩ | kilohms | V | volts |
| lb. | pounds | W | watts |

Other abbreviations used in developer notes include these:

| | |
|---|---|
| $*n* | hexadecimal value *n* |
| ADB | Apple Desktop Bus |
| ADC | Apple digital connector |
| AGP | accelerated graphics port |
| ATA | advanced technology attachment |
| ATAPI | advanced technology attachment, packet interface |
| AV | audiovisual |
| CAS | column address strobe |
| CDDA | compact disc digital audio |
| CD-ROM | compact disc read-only memory |
| CLUT | color lookup table |
| CRM | Communications Resource Manager |
| DAC | digital to analog converter |
| DBDMA | descriptor-based direct memory access |
| DDC | display data channel |
| DIMM | dual inline memory module |
| DIN | Deutsche Industrie Norm |
| DLPI | Data Link Provider Interface |
| DMA | direct memory access |
| DRAM | dynamic random-access memory |
| DVD | 12 cm optical storage system with 4 GB capacity |
| DVD-ROM | DVD read-only memory |
| DVD-RAM | DVD that is both readable and writeable |
| DVI | Digital Visual Interface |

| | |
|---|---|
| EDO | extended data out DRAM device type |
| EMI | electromagnetic interference |
| ESDRAM | enhanced synchronous dynamic random-access memory |
| FWIM | FireWire interface module |
| G3 | Generation 3, the third generation of PowerPC microprocessors, including the PPC 740 and PPC 750 |
| G4 | Generation 4, the fourth generation of PowerPC microprocessors, incorporating AltiVec technology |
| GCR | group code recording |
| HID | human interface device, a class of USB devices |
| $I^2C$ | same as IIC |
| $I^2S$ | same as IIS |
| IC | integrated circuit |
| IEEE | Institute of Electrical and Electronics Engineers |
| IEEE 1394 | the official specification for FireWire |
| IIC | inter-integrated circuit (an internal control bus) |
| IIS | inter IC sound bus |
| I/O | input/output |
| IR | infrared |
| IrDA | Infrared Data Association |
| ISO | International Organization for Standardization |
| JEDEC | Joint Electronics Devices Engineering Council |
| L2 | level 2, used in reference to level of cache |
| LAN | local area network |
| MAC | media access controller |
| Mac OS | Macintosh Operating System |
| MESH | Macintosh enhanced SCSI hardware |
| MMU | memory management unit |
| MPEG | Motion Picture Experts Group |
| NTSC | National Television Standards Committee (the standard system used for broadcast TV in North America and Japan) |

| | |
|---|---|
| OHCI | Open Host Controller Interface |
| PAL | Phase Alternating Line system (the standard for broadcast TV in most of Europe, Africa, South America, and southern Asia) |
| Pel | pixel element; an individual red, green, or blue value of an RGB pixel |
| PCI | Peripheral Component Interconnect |
| PGA | pin grid array |
| PHY | physical layer |
| PIO | polled input/output |
| RAM | random-access memory |
| RAS | row address strobe |
| RAVE | Rendering Acceleration Virtual Engine |
| RBC | reduced block commands |
| RGB | a video signal format with separate red, green, and blue components |
| RISC | reduced instruction set computing |
| ROM | read-only memory |
| SBP | Serial Bus Protocol |
| SCSI | Small Computer System Interface |
| SCC | serial communications controller |
| SDRAM | synchronous dynamic random access memory |
| SECAM | the standard system used for broadcast TV in France and the former Soviet countries |
| SIMM | single inline memory module |
| SGRAM | synchronous graphics random access memory |
| SO-DIMM | small outline dual inline memory module |
| SRAM | static random access memory |
| S-video | a type of video connector that keeps luminance and chrominance separate; also called a Y/C connector |
| USB | Universal Serial Bus |
| TMDS | transition minimized differential signaling |
| VESA | Video Electronics Standards Association |

| | |
|---|---|
| VRAM | video RAM; used for display buffers |
| Y/C | a type of video connector that keeps luminance and chrominance separate; also called an S-video connector |
| YUV | a video signal format with separate luminance and chrominance components |

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This Apple manual was written, edited, and composed on a desktop publishing system using Apple Macintosh computers and FrameMaker software. Line art was created using Adobe™ Illustrator and Adobe Photoshop.

Text type is Palatino® and display type is Helvetica®. Bullets are ITC Zapf Dingbats®. Some elements, such as program listings, are set in Adobe Letter Gothic.

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