Macintosh® Quadra 900

Developer Note

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Developer Technical Publications

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Preface

About this note

This developer note describes the Macintosh Quadra 900 computer, the new high-performance model in the Macintosh family of computers. Using an MC68040 microprocessor and a new floor-standing case, the Macintosh Quadra 900 achieves higher performance than any previous Macintosh computer.

This developer note has three chapters. Chapter 1, "Macintosh Quadra 900 Hardware," describes the main features and emphasizes the circuitry and the new case design of the machine. Chapter 2, "Expansion Interface," describes the expansion capabilities of the machine. Chapter 3, "ROM Features," describes the new features of the ROM software.

It is assumed that hardware and software developers are already familiar with both the functionality and programming requirements of Macintosh computers. If you are unfamiliar with the Macintosh or would simply like more technical information on the hardware, you may want to obtain copies of related technical manuals. For information on how to obtain these manuals, see the following section.

For more information

To supplement the information in this document, hardware and/or software developers might wish to obtain related documentation such as the *Guide to the Macintosh Family Hardware,* second edition; *Designing Cards and Drivers for the Macintosh Family,* second edition; and *Inside Macintosh,* Volumes I through VI. Copies of these technical manuals are available through APDA (Apple Programmers and Developers Association).

Chapter 3, "ROM Features," refers to Macintosh Technical Notes 261 and 282. Macintosh Technical Notes are also available through APDA

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You may also wish to refer to the NuBus specification, *IEEE Standard for a Simple 32-bit Backplane Bus: NuBus,* IEEE Std. 1196-1987, and to the NuBus '90 proposal, *IEEE Standard for a Simple 32-bit Backplane Bus: NuBus,* IEEE Std. R1196-R-1990. You can obtain those documents by mail from IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854, or telephone 201-981-0060.

Chapter 1 Macintosh Quadra 900 Hardware

This chapter describes the main features of the Macintosh Quadra 900 computer, with emphasis on new circuitry features and case design.

Introduction

The Macintosh Quadra 900 computer is the most powerful member of the new, high-performance Macintosh Quadra family. Another new computer in the Macintosh Quadra family, the Macintosh Quadra 700, is functionally similar to the Macintosh Quadra 900 but has a different case design and a reduced feature set. A brief comparison of the two machines is provided later in this chapter. For more information on the Macintosh Quadra 700, see the *Macintosh Quadra 700 Developer Note.*

The Macintosh Quadra 900 includes several advanced features that improve its performance over that of the Macintosh II computer family. Foremost of those features are the Motorola MC68040 microprocessor and built-in video display hardware. The MC68040 has built-in caches, memory management unit (MMU), and a floating-point unit (FPU). The computer's built-in video hardware provides 24-bit color and performance approaching that of the Macintosh Display Card 8•24GC.

Improved I/O features also contribute to the higher performance of the Macintosh Quadra 900 computer. Like the Macintosh IIfx, the Macintosh Quadra 900 has intelligent I/O processors (IOPs) on the ports for the floppy disk, Apple Desktop Bus (ADB), and serial I/O to relieve the main processor of routine I/O tasks. The SCSI (Small Computer System Interface) interface uses separate ICs for internal and external devices.

To enhance the overall capabilities of the Macintosh Quadra 900, expansion opportunities are provided by five NuBus™ slots and one processor-direct slot (PDS). Chapter 2 provides a detailed discussion of the Macintosh Quadra 900 computer's expansion interface.

The Macintosh Quadra 900 computer has a new, larger case that stands on the floor. This new case provides space for more peripheral devices than was provided in the standard Macintosh II case.

Summary of hardware features

The hardware features of the Macintosh Quadra 900 computer include

- a Motorola MC68040 microprocessor running at 25 MHz
- a new, larger case, designed to stand on the floor
- support for as many as four internal mass-storage devices, including two with removable media
- up to 64 MB of dynamic RAM in 30-pin SIMMs (Single Inline Memory Modules) in four separate memory banks
- built-in video hardware with direct-access frame buffer using separate video RAM
- a dual-channel SCSI interface for faster internal and external SCSI devices
- intelligent I/O processors for floppy disk, ADB, and serial I/O ports
- built-in support for Ethernet by way of Apple AUI (AAUI)
- an Apple SuperDrive high-density floppy disk drive with 1.44 MB capacity
- five NuBus expansion slots with NuBus '90 features and space for oversized
  NuBus cards
- a processor-direct slot for lhigh-performance hardware expansion
- improved sound capability with integration of sound from CD-ROM
- a key lock for security
- a larger power supply with capacity of 300 watts

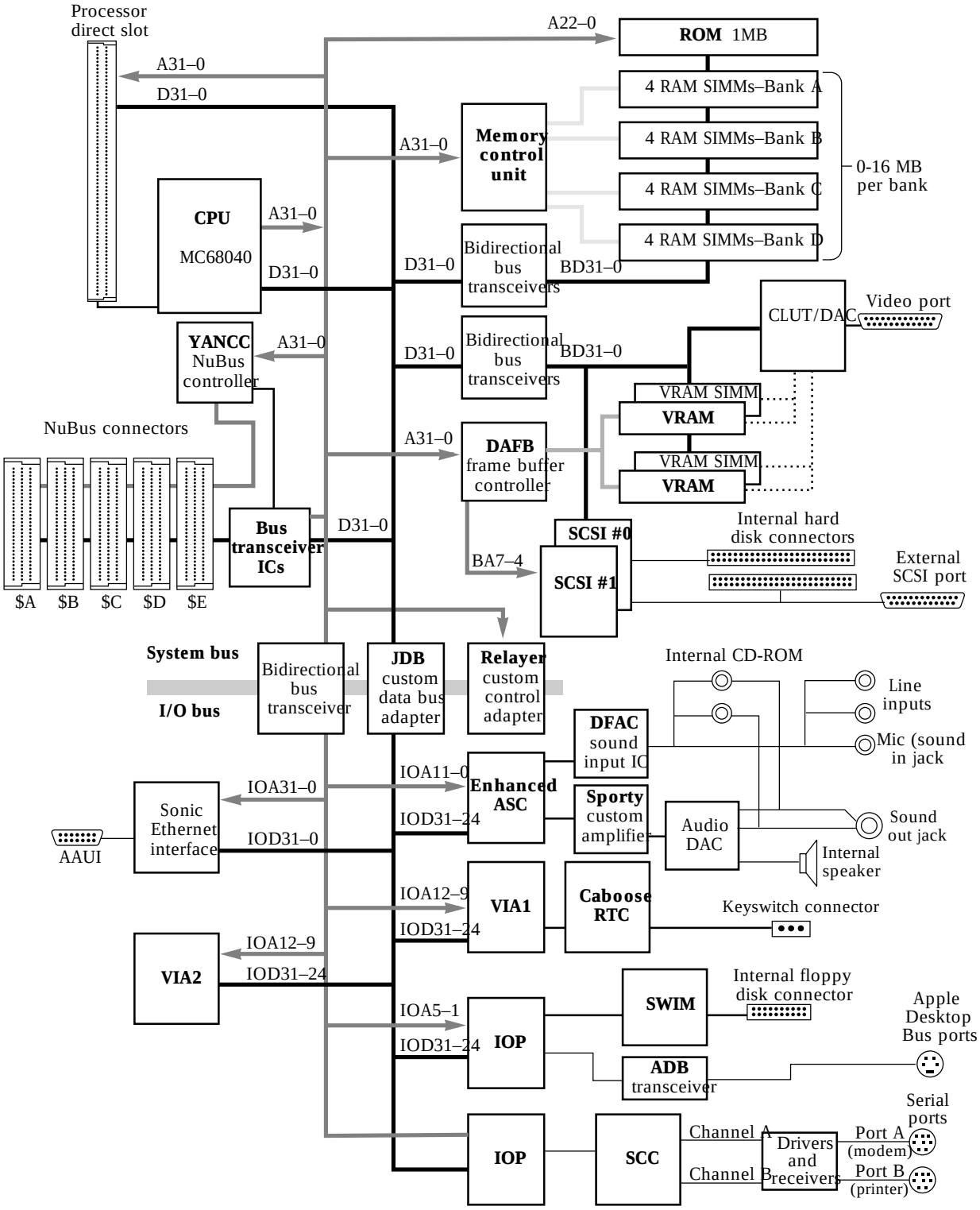
Design architecture

The circuitry of the Macintosh Quadra 900 computer has many new features along with older features that it shares with the Macintosh IIci and Macintosh IIfx computers. This section describes the circuit design of the Macintosh Quadra 900, with emphasis on the custom integrated circuits that implement its new features.

Figure 1-1 is a simplified block diagram of the Macintosh Quadra 900 computer, showing the major hardware components and the address and data buses.

Certain components appear for the first time in the Macintosh Quadra 900: the MC68040 microprocessor, several new custom ICs, the built-in video hardware, and the 68040 PDS connector.

- **Figure 1-1** Block diagram of the Macintosh Quadra 900 computer


Processor direct slot
A22–0
ROM 1MB
A31–0
D31–0
4 RAM SIMMs–Bank A
4 RAM SIMMs–Bank B
4 RAM SIMMs–Bank C
4 RAM SIMMs–Bank D
0-16 MB per bank
A31–0
Memory control unit
CPU
MC68040
A31–0
D31–0
D31–0
Bidirectional bus transceivers
BD31–0
CLUT/DAC
Video port
YANCC NuBus controller
A31–0
D31–0
Bidirectional bus transceivers
BD31–0
VRAM SIMM
VRAM
NuBus connectors
A31–0
DAFB frame buffer controller
VRAM SIMM
VRAM
$A
$B
$C
$D
$E
Bus transceiver ICs
D31–0
SCSI #0
Internal hard disk connectors
BA7–4
SCSI #1
External SCSI port
System bus
I/O bus
Bidirectional bus transceiver
JDB custom data bus adapter
Relayer custom control adapter
Internal CD-ROM
Line inputs
Mic (sound in jack
DFAC sound input IC
IOA11–0
Enhanced ASC
IOA31–0
Sonic Ethernet interface
IOD31–24
Sporty custom amplifier
Audio DAC
Sound out jack
Internal speaker
AAUI
IOD31–0
IOA12–9
VIA1
Caboose RTC
IOD31–24
Keyswitch connector
IOA12–9
VIA2
IOD31–24
IOA5–1
IOP
SWIM
Internal floppy disk connector
IOD31–24
ADB transceiver
Apple Desktop Bus ports
Serial ports
IOP
SCC
Channel A
Channel B
Drivers and receivers
Port A (modem)
Port B (printer)

There are three buses in the Macintosh Quadra 900 computer: the system bus, the I/O bus, and NuBus.

The system bus connects directly to the pins of the MC68040 microprocessor and runs at the processor's clock rate, 25 MHz. Five controller ICs are connected to the system bus: the MCU (Memory Control Unit); YANCC, the NuBus controller; DAFB, the frame-buffer controller; and the two SCSI controllers.

The I/O bus in the Macintosh Quadra 900 computer is similar to the I/O bus in the Macintosh IIfx computer. The I/O bus in the Macintosh Quadra 900 computer runs at a clock rate of 15.6672 MHz. The controller ICs that are connected to the I/O bus include new custom ICs along with ICs originally designed for the Macintosh IIfx, such as
the IOPs.

The NuBus, the industry-standard expansion bus used in all Macintosh II–family computers, runs at a clock rate of 10 MHz. The NuBus in the Macintosh Quadra 900 computer includes several features of NuBus '90, including a clock signal at 20 MHz, twice the normal rate. NuBus '90 is the 1990 proposal for revision of the IEEE standard for the NuBus (IEEE Std. R1196-R-1990). For more information about NuBus, see Chapter 2,
"The Expansion Interface."

MC68040 microprocessor

The Macintosh Quadra 900 computer is the first Macintosh model to use the MC68040 microprocessor. The MC68040 is the most powerful member of the 68000 family, with performance approximately three times that of an MC68030 with the same clock speed. While the MC68040 is upwardly compatible with application software written for the MC68020 and MC68030, it also has many new features that contribute to its increased processing power.

The new features of the MC68040 include

- a redesigned and optimized integer unit
- a built-in floating-point unit (FPU),
- built-in memory management units (MMUs), one for instructions and one for data

- built-in instruction and data caches, 4 KB each

The MC68040 is different in many ways from the MC68020 and MC68030. For example, the built-in floating-point unit of the MC68040 is not the same as the MC68881 FPU; similarly, the built-in PMMU is not the same as the MC68851 MMU or the built-in MMU in the MC68030. Also, the instruction and data caches in the MC68040 use a new mode called CopyBack mode. For information about these differences and the way they are reflected in the new ROM software developed for the Macintosh Quadra 900, see Chapter 3, "ROM Features."

♦ *Note:* The MC68040 has another new feature called cache snooping. That feature is not used in the Macintosh Quadra 900 computer and is not supported by the software. Devices that transfer data on the system bus, such as PDS bus masters, must drive the snoop control pins to indicate no snooping.

Custom ICs

The Macintosh Quadra 900 computer incorporates many VLSI (very large scale integration) ICs. Some of those ICs, such as the Motorola MC68040, are industry-standard designs, and others are Apple custom ICs. Of the Apple custom ICs, some are also used in earlier Macintosh computers; others are newly designed for the Macintosh Quadra 900 computer. The new Apple custom ICs are described in the sections that follow.

The Apple custom ICs that the Macintosh Quadra 900 computer shares with earlier Macintosh models include

- CLUT/DAC (color look-up table and digital-to-analog converter) IC developed by Apple and used in the Macintosh Display Card 4•8, 8•24, and 8•24GC
- DFAC (Digitally Filtered Audio Chip), the sound input and filter IC first used in the Macintosh LC
- IOP, the I/O processors first used in the Macintosh IIfx

- SWIM (Super Woz Integrated Machine), the IC that supports the SuperDrive
high-density floppy disk drive

The Apple custom ICs that are newly designed for the Macintosh Quadra 900 computer are

- Enhanced ASC (Apple Sound Chip), a custom IC that replaces the Apple Sound Chip
- Caboose, a custom processor that manages the keyswitch, system power, the real-time clock, and parameter RAM
- DAFB (Direct Access Frame Buffer), an IC that connects directly to the system bus and controls the video RAM (frame buffer)
- JDB (Junction Data Bus), one of two ICs making up the I/O Adapter, connecting the data signals from the system bus and the I/O bus
- MCU, a custom IC that connects to the system bus and controls access to ROM and RAM supporting the main processor's burst-mode data transfers
- Relayer, one of two ICs making up the I/O Adapter, controlling the bus buffers and providing bus arbitration logic
- Sporty, a custom IC that provides sound output amplification functions
- YANCC (Yet Another NuBus Controller Chip), a custom IC that controls the
NuBus interface

Other ICs—third-party products, not Apple designs—include

- SCSI interface ICs: two NCR 53C96 ICs
- Sonic, the DP83932 Ethernet controller IC made by National Semiconductor
- two VIAs like the ones in earlier members of the Macintosh II family

I/O bus adapter ICs: JDB and Relayer

The I/O bus enables the Macintosh Quadra 900 computer to use the same I/O device controllers used in previous Macintosh computers. The I/O bus clock runs at 15.6672 MHz and is completely asynchronous to the system bus clock.

The I/O bus adapter is made up of two ICs named JDB (Junction Data Bus) and Relayer. Two ICs are used because of the high pin count required.

The functions of the Relayer IC include

- generating chip select and DSACK signals for devices on the I/O bus
- converting timing signals between the system bus and the I/O bus
- arbitrating between the system bus and the I/O bus
- acting as watchdog for bus activity and timeout
- controlling the address-bus transceiver ICs
- generating the clock signal for the VIA ICs

The functions of the JDB IC include

- controlling the data path (dynamic bus sizing and data byte lane routing)
- synchronizing and distributing the reset signals

The ICs making up the I/O bus adapter contain no programmable registers and do not require support from the system software.

Memory Control Unit

The MCU connects to the system bus and provides control and timing signals for RAM and ROM. The MCU supports all types of MC68040 memory access, including burst modes. Figure 1-2 is a simplified address map for the Macintosh Quadra 900 computer showing the I/O space in detail.

ROM control

The MCU controls the Macintosh Quadra 900 computer's 1 MB ROM, which consists of two 4-Mbit ROMs (each ROM is a 256K x 16-bit, 150-ns device). A ROM SIMM socket is available for future expansion; however, when a ROM SIMM is installed in this socket, the on-board ROM will be automatically disabled.

When the computer is reset, the MCU maps ROM addresses into memory beginning at address $0000 0000 and disables the system RAM. As soon as the ROM code addresses the normal ROM space ($4000 0000), the MCU automatically remaps the ROM to its normal addresses and restores RAM addressing starting at $0000 0000.

RAM control

The MCU controls four banks of dynamic RAM. Each bank accepts standard 80-ns SIMMs containing 1 MB, 4 MB, or 16 MB, giving total memory sizes from 4 MB to 64 MB.

- *Note:* Each bank of main RAM occupies 64 MB of physical address space.

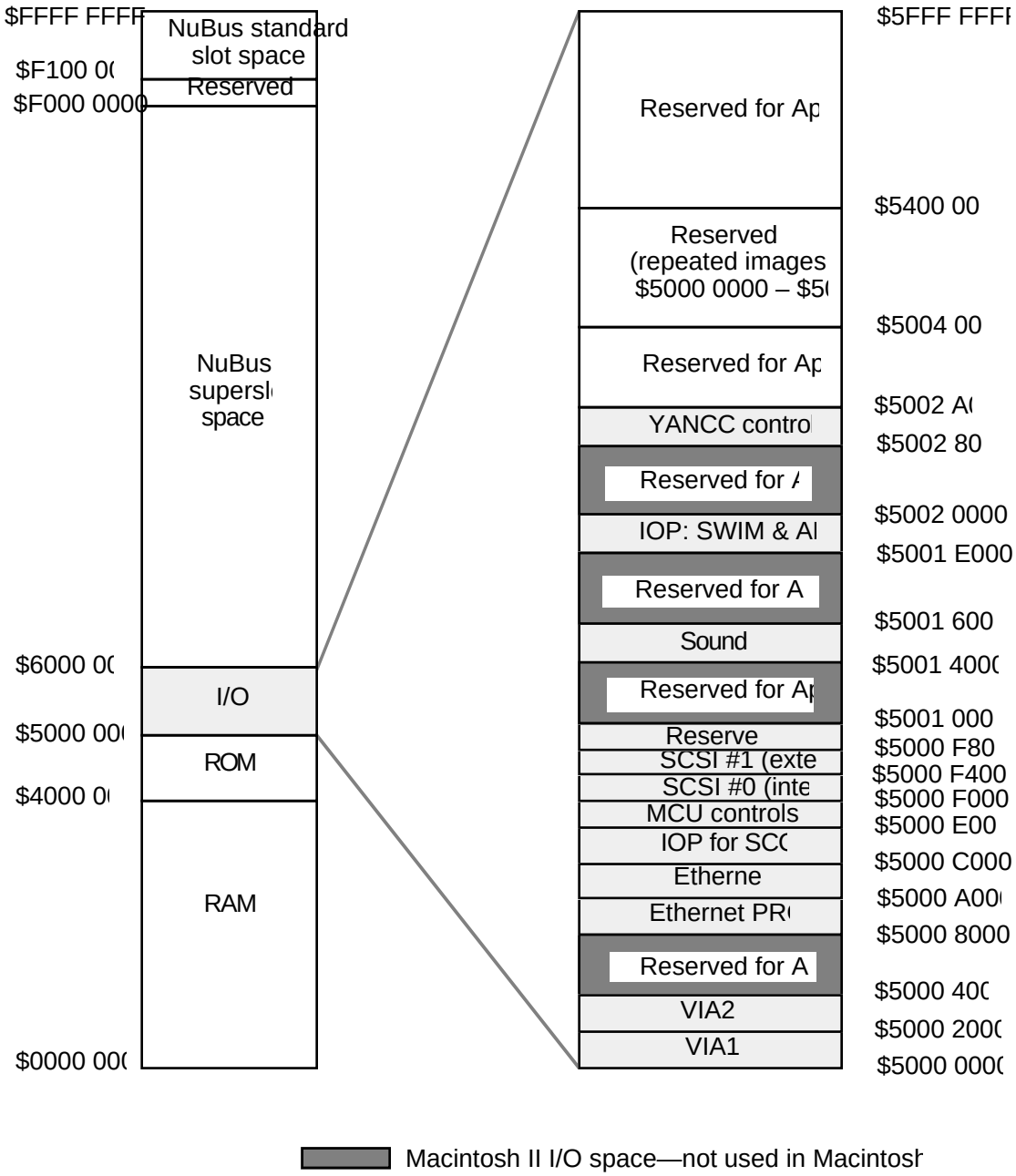
The MCU contains registers that the system software uses to set the starting address of each bank of memory. At startup time, the system software determines the sizes of the banks and assigns the bank starting addresses so that the banks occupy contiguous memory spaces.

SCSI controller ICs

In the Macintosh Quadra 900 computer, the SCSI bus is divided into internal and external buses, each controlled by its own IC. Both ICs are NCR 53C96 devices.

The internal and external SCSI buses are logically connected but electrically separate. The external bus is electrically isolated from the internal bus so that changes in external cabling and termination have no effect on the performance of the internal SCSI devices.

- **Figure 1-2** Simplified I/O address map for the Macintosh Quadra 900 computer



The cabling and termination of the internal SCSI bus are optimized so that the 53C96
that controls the internal bus can support data transfers at a faster rate—up to 5 MB/sec. Because the external cabling and termination are less predictable, the 53C96 that controls the external SCSI bus may run more slowly than the 53C96 that controls the internal
SCSI bus.

NuBus controller IC: YANCC

In the Macintosh Quadra 900 computer, three chips comprise the interface between the system bus and the NuBus: the YANCC IC and two 16-bit transceiver ICs. The transceivers are the same as those in the Macintosh IIci.

Unlike the NuBus controllers in previous Macintosh computers, the YANCC IC generates an interrupt when there is an error involving the write buffer. Software controls this interrupt by means of a control and status register in the YANCC. See Figure 1-3 for the simplified NuBus address map.

The YANCC IC maps certain system bus cycles to NuBus cycles and certain NuBus cycles to system bus cycles. The features of the YANCC IC include

- support for all types of single data transfers in either direction
- a buffer, one long word deep, for pending writes from the MC68040 to the NuBus
- support for block move transfers between NuBus masters and main memory
- support for pseudoblock transfers between the MC68040 and NuBus slaves
- support for some new functions defined in the NuBus ’90 specification

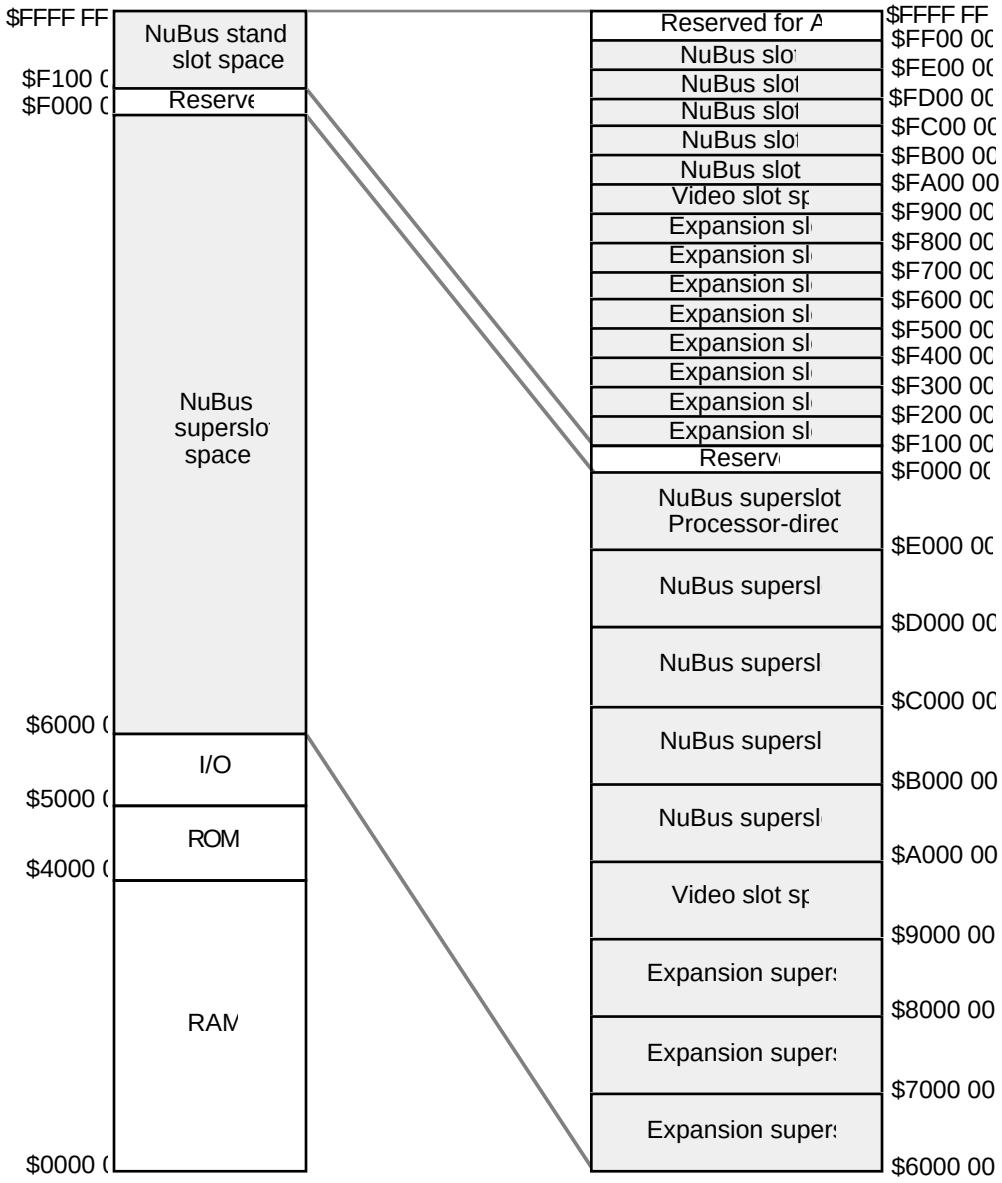
Video frame-buffer controller IC: DAFB

The built-in video hardware in the Macintosh Quadra 900 computer provides high-performance graphics on all current Macintosh monitors. The video hardware is built around a video frame buffer controlled by the DAFB (Direct Access Frame Buffer) IC.

The video frame buffer comprises four banks of video RAM (VRAM); the basic configuration has VRAM installed in two of the four banks. That configuration supports 8 bits per pixel on all Apple monitors (12-inch to 21-inch, monochrome and RGB) and on NTSC and PAL monitors, using Apple convolution. The basic configuration also supports VGA monitors.

The basic VRAM configuration supports 24 bits per pixel on the 12-inch RGB monitor. By installing VRAM SIMMs into the other two banks, the user can expand the frame buffer to support 24 bits per pixel for the 13-inch monitor.

- **Figure 1-3** Simplified NuBus address map for the Macintosh Quadra 900 computer



The video hardware in the Macintosh Quadra 900 computer provides graphics performance approaching that of the Macintosh Display Card 8•24GC. That card is still faster for certain graphics operations, but not all applications benefit from the acceleration it provides. Because the frame buffer in the Macintosh Quadra 900 computer is connected directly to the system bus, it speeds up all applications, even those that don't use QuickDraw. The control registers in the DAFB IC and the frame-buffer VRAM are mapped into the memory locations that were assigned to NuBus slot $9 in earlier models.

Sound ICs: DFAC, Enhanced ASC, and Sporty

The Macintosh Quadra 900 computer uses a new sound system. Its features are similar to the features of the sound interface in the Macintosh LC and the Macintosh IIsi. The features of the Macintosh Quadra 900 sound interface include

- the ability to record monophonic sound from microphone input, audio line inputs, or internal CD-ROM playback.
- the ability to play sound from internal CD-ROM
- the ability to play 8-bit sound files
- the ability to mix sound played from internal CD-ROM with sound from sound files

Three Apple custom ICs plus a digital-to-analog converter provide the sound interface:

- DFAC, which provides sound input and an antialiasing filter
- Enhanced ASC, an updated version of the Apple Sound Chip
- Sporty, a custom IC that replaces the two Sony sound ICs
- an external digital-to-analog converter (DAC)

The DFAC is an Apple custom IC that is also used in the Macintosh LC. The DFAC IC includes the antialiasing filter and analog-to-digital converter (ADC) for sound input. It also contains a digital filter for conditioning output data before it is sent to the DAC.

For sound output, an external DAC provides higher-quality sound than that generated by the PWM system used in earlier Macintosh models. The Sporty custom IC replaces the two Sony ICs used in earlier models and provides better sound quality: less noise and distortion. Like the Sony ICs it replaces, the Sporty IC also contains digital attenuators.
A separate amplifier with power output of 2 watts drives the larger speaker used in the Macintosh Quadra 900 computer.

The following section describes the new floor-standing case of the Macintosh Quadra 900 computer. Chapter 2 describes the expansion capabilities of the machine.

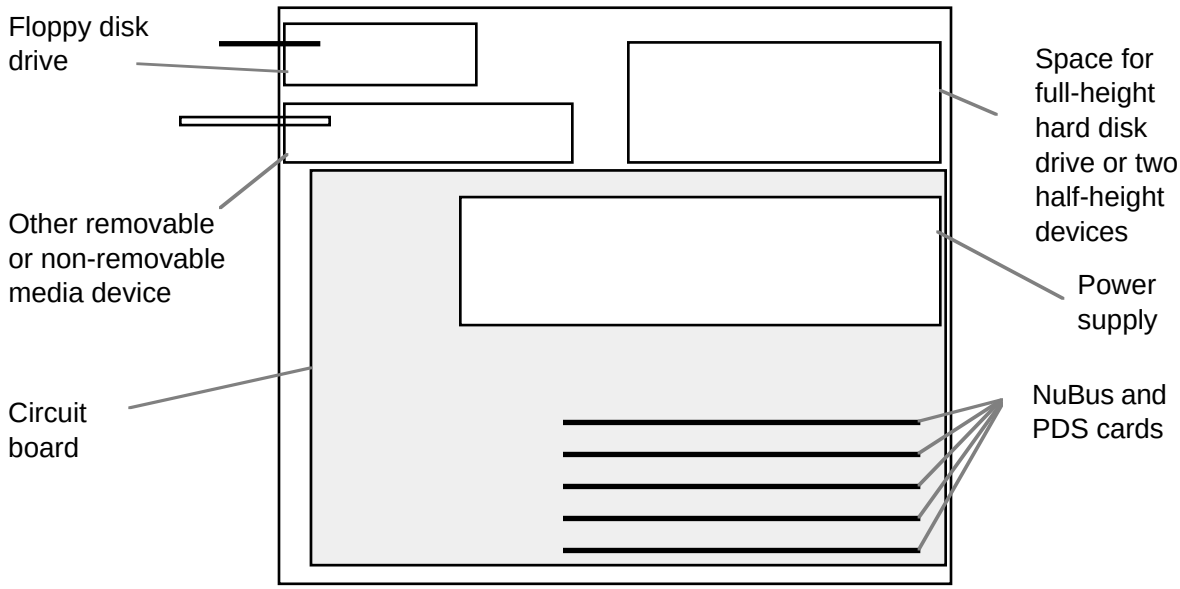
Floor-standing case

The Macintosh Quadra 900 computer has a new case designed to stand on the floor
(see Figure 1-4). The design provides many new features, including

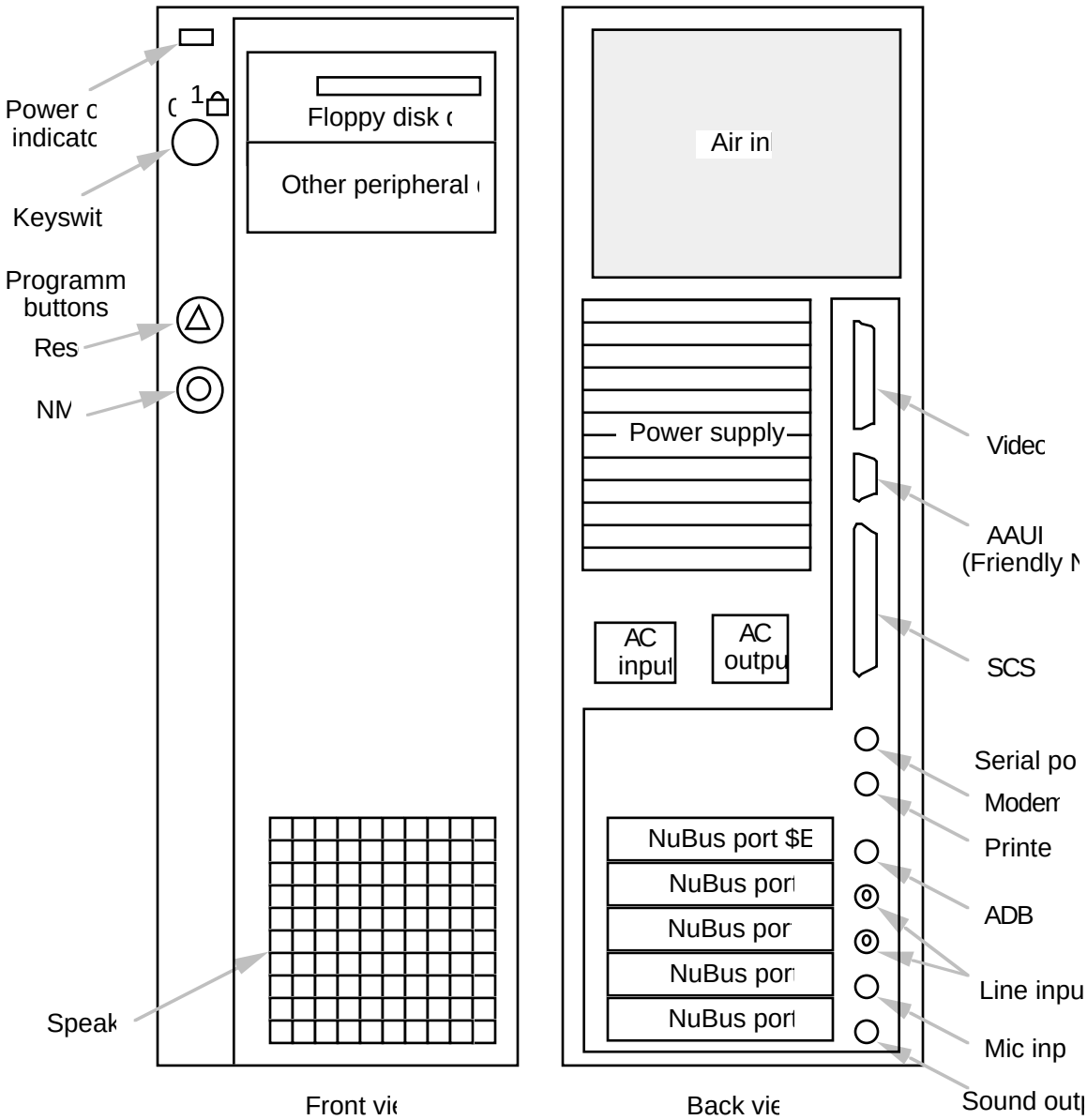
- a floor-standing case for more space and better cooling
- space for as many as four internal peripheral devices, including full-height disk drives and removable media
- provision for an internal CD-ROM player, integrated with system sound features
- a larger power supply to support internal devices and higher-power NuBus cards
- a locking keyswitch for security and operation as a server
- sound input for microphone (included) and line signals

Figure 1-4 shows a simplified side view of the new case with the locations of the peripheral devices, power supply, and expansion cards. Figure 1-5 shows front and back views with the positions of the controls and connectors.

- **Figure 1-4** Diagram of floor-standing case, showing major components



- **Figure 1-5** Front and back views of the Macintosh Quadra 900 computer



Internal mass-storage devices

The floor-standing case provides flexibility for internal mass-storage devices. There are four half-high mounting locations. Two of the four are in the front of the case, where they are accessible for removable media. Any of the four locations can accommodate either 3.5-inch or 5.25-inch SCSI hard disk drives.

A hard disk drive for the Macintosh Quadra 900 computer can be any 3.5-inch or 5.25-inch half-height device or a 5.25-inch full-height device, allowing the Macintosh Quadra 900 to accommodate any current Apple disk drive—20 MB, 40 MB, 80 MB, or 160 MB—as well as future Apple products or third-party devices. Third-party full-height drives are available with even higher capacities.

The upper front location will normally be filled with a 1.44 MB SuperDrive disk drive. The lower front location can accommodate tape, magneto-optical, or similar removable media devices. The lower front location can also be used for a CD-ROM drive.

SCSI connectors

The SCSI interface in the Macintosh Quadra 900 computer is designed with dual controller ICs, one for internal devices and the other for external devices. For more information on the operation of the dual controllers, see "SCSI Controller ICs" earlier in this chapter.

The Macintosh Quadra 900 includes two internal 50-pin SCSI connectors and one
external DB-25 SCSI connector. The SCSI connectors are identical to those used on Macintosh II–family computers. Table 1-1 shows the pinouts for the internal and external SCSI connectors.

- *Note:* SCSI devices designed for external use should be terminated if they are the last device on the chain. SCSI devices designed for internal use should not be terminated.

- **Table 1-1** Pinouts for internal and external SCSI connectors

Internal (50-pin)	External (25-pin)	Signal name
48	1	/REQ
42	2	/MSG
46	15	/C/D
50	3	/I/O
40	4	/RST
32	17	/ATN
38	5	/ACK
36	6	/BSY
44	19	/SEL
18	20	/DBP
2	8	/DB0
4	21	/DB1
6	22	/DB2
8	10	/DB3
10	23	/DB4
12	11	/DB5
14	12	/DB6
16	13	/DB7
26	25	TPWR
Pins 20, 22,24, 26, 28, 30, 34, and all odd pins except pin 25 (30 total)		7, 9, 14, 16, 18, and 24 GND

Floppy disk connector

A single SWIM chip controls the internal SuperDrives. A 20-pin connector provides the signal interface between the SWIM chip and the drive. Table 1-2 shows the pinout for the floppy disk connector.

- **Table 1-2** Pinout for floppy disk internal connector

Pin number	Signal name	Signal description
1	GND	Ground
2	PH0	Phase 0: state-control line
3	GND	Ground
4	PH1	Phase 1: state-control line
5	GND	Ground
6	PH2	Phase 2:state-control line
7	GND	Ground
8	PH3	Phase 3: register write strobe
9	n.c.	Not connected
10	/WRREQ	Write data request
11	+5V	+5 V
12	SEL	Head select
13	+12V	+12 V
14	/ENBL	Drive enable
15	+12V	+12 V
16	RD	Read data
17	+12V	+12 V
18	W R	Write data
19	+12V	+12 V
20	n.c.	Not connected

Internal CD-ROM integration

One of the internal storage devices in the Macintosh Quadra 900 computer can be a
CD-ROM drive, installed at the front for media access. The drive connects to the internal SCSI bus through a cable attached to one of the two internal SCSI connectors, and an additional cable takes the audio signals from the CD-ROM to the main circuit board. This integration of the audio signals into the computer provides three functions that are important for multimedia applications:

- ability to play audio from the CD-ROM through the internal sound system
- ability to mix audio from the CD-ROM with computer-generated sound
- ability to perform digital recording of audio from the CD-ROM

Power supply

The power supply adapts automatically to the AC voltage that is applied. The
localization package for the computer will include the appropriate power cord for the destination country.

The power supply includes a 120-mm (4.72-in.) fan that provides quiet cooling for the entire system. The power supply also includes a switched convenience receptacle to provide power for the monitor.

Table 1-3 shows the minimum, maximum, and peak ratings for the power supply. The output labeled +5V TRKL is a trickle supply that is available whenever the computer is plugged in. That output provides power for the parameter RAM and the power-on logic, along with standby power for the NuBus cards. The +12-V output is designed with a peak capacity high enough to meet the combined current demands made by all the peripheral devices turning on at the same time.

- **Table 1-3** Power supply ratings

Load	+5 V	+5V TRKL	+12 V	–12 V	Total power	
Minimum W		5 A	1 mA	150 mA	50 mA	27.5
Maximum W		33 A	125 mA	9 A	1 A	292
Peak	33 A	125 mA	20 A*	1 A	424 W*	

*For a period of 12 seconds maximum

Keyswitch

The keyswitch has three positions: OFF, ON, and SECURE. The key can be removed while the switch is in any of the three positions. The operation of the keyswitch is designed to provide a first level of security for users who wish to use it, without being inconvenient for those who don't.

Keyswitch OFF position

When the keyswitch is in the OFF position, the computer cannot be turned on. Moving the keyswitch from either the ON or SECURE position to the OFF position turns the machine off.

♦ **Warning** Turning the keyswitch to OFF when the computer is running turns the power off immediately: the system software does not have a chance to close files. If you turn the machine off by turning the keyswitch to OFF, you can lose data. ♦

Keyswitch ON position

When the keyswitch is in the ON position, the computer can be turned on from the keyboard and turned off by choosing the Shut Down menu item. When the keyswitch is in the ON position, the user controls the power the same way as on any other computer in the Macintosh II family.

Keyswitch SECURE position

When the keyswitch is in the SECURE position, the ADB devices and the floppy disk are disabled. When power is applied to the computer while the keyswitch is in the SECURE position, the computer automatically starts up. The SECURE position is intended for situations involving remote access or in which the computer acts as a network server.

Programmer's buttons

Like many other models in the Macintosh family, the Macintosh Quadra 900 computer has two pushbuttons, the reset button and the NMI button. The recessed edge of the case protects the buttons from being accidentally pressed.

♦ *Note:* The reset and NMI buttons remain active when the keyswitch is in the SECURE position.

Microphone and Mic In connector

The Macintosh Quadra 900 computer has a Mic In connector in the back, and a microphone is included with the computer. The microphone is similar to the one provided with the Macintosh IIsi and the Macintosh LC, but it has a longer cable to allow it to reach the floor-standing case.

♦ **Warning** Do not plug any device other than the Macintosh microphone into the Mic In connector on the Macintosh Quadra 900 computer. That connector includes +8 volts on one of its pins. Plugging a device such as a standard microphone, headphone, or speaker into the Mic In connector could cause damage to the device. ♦

Audio Line In connectors

The audio Line In connectors are standard phono connectors. They are intended for users who wish to use the computer to sample line-level devices such as home stereo systems. The signals from the Line In connectors are internally mixed to a single (monophonic) audio signal; that signal is combined with the input from the Mic In connector and then sent to the sound input circuit.

- *Note:* Even though there are two Line In connectors, the stereo channels are mixed into a single monophonic signal; stereo information is lost. The computer has two connectors for the user's convenience and so that an external mixer is not needed when connecting the computer to the most common type of consumer audio equipment.

Sound Out connector and speaker

The Sound Out connector on the Macintosh Quadra 900 computer is similar to the one on the Macintosh II and has the same electrical characteristics.

The audio amplifier for the internal speaker is more powerful than those on other models so that it can drive the speaker at higher sound levels. The higher levels are required because the computer is normally on the floor and thus farther from the user.

Ethernet connector

The Ethernet connector on the Macintosh Quadra 900 computer is the Apple AUI (AAUI) connector, which accepts any FriendlyNet adapter. There is a different FriendlyNet adapter for each of the different kinds of Ethernet standard cable: the AUI (thick) cable, the CheaperNet (thin) cable, and the 10BaseT (twisted pair) cable.

Comparison with the Macintosh Quadra 700 computer

Table 1-4 compares the features of the Macintosh Quadra 900 and the Macintosh Quadra 700 computers. For detailed information on the Macintosh Quadra 700 computer, refer to the *Macintosh Quadra 700 Developer Note.*

- **Table 1-4** Feature comparison of Macintosh Quadra 900 and Macintosh Quadra 700 computers

Feature	Macintosh Quadra 900	Macintosh Quadra 700
Memory	4 banks of DRAM (all on SIMMs)	2 banks of DRAM (1 bank soldered; 1 bank SIMMs)
SCSI	Dual SCSI controllers (1 internal and 1 external); Room for 4 internal SCSI devices, including any combination of 3.5-inch and 5.25-inch devices	Single SCSI controller (for both internal and external SCSI devices) and room for one internal 3.5-inch hard disk
NuBus	5 slots, 19 W power per slot (or two 25 W slots and three 15 W slots; or a total not to exceed 95 W); both oversize and standard NuBus cards allowed	2 slots, 15 W per slot (or a total not to exceed 30 W); only standard size NuBus cards allowed
PDS	O1 PDS slot (cards will also work in Macintosh Quadra 700)	1 PDS slot (cards will also work in Macintosh Quadra 900)
Floppy	SWIM/IOP	SWIM
Serial ports	SCC/IOP	SCC
ADB	Same as Macintosh IIfx	Same as Macintosh IIci
Video	2 banks of VRAM soldered; 2 banks for expansion VRAM	1 bank of VRAM soldered; 3 banks for expansion VRAM

Chapter 2 **Expansion Interface**

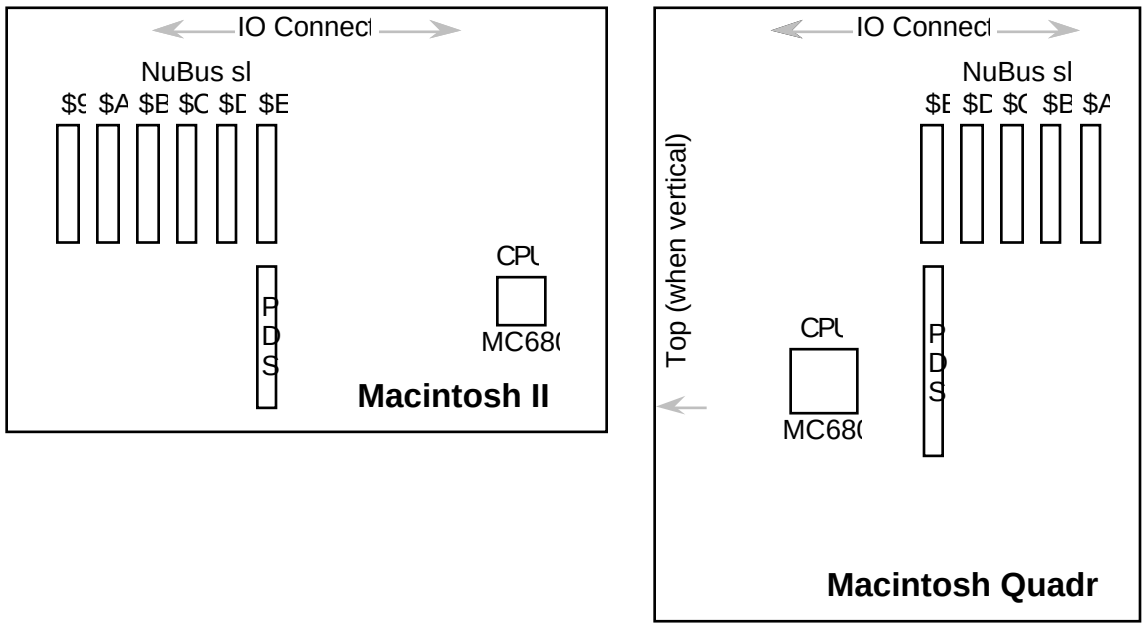
This chapter describes the NuBus and processor-direct slot expansion capabilities of the Macintosh Quadra 900 computer.

Expansion slots

The Macintosh Quadra 900 computer has five NuBus slots and one PDS (processor-direct slot). The PDS is located in line with NuBus slot $E and uses the same opening in the back. The use of a PDS card precludes the use of a NuBus card in slot $E.

Figure 2-1 shows the arrangement of the expansion slots on the main circuit boards of the Macintosh IIfx and Macintosh Quadra 900 computers. Notice the differences in the arrangement of the slots in the two computers.

- **Figure 2-1** Arrangement of the expansion slots



NuBus slots

The Macintosh Quadra 900 computer has five NuBus slots. Those NuBus slots are different from those on the other modular Macintosh computers in three ways:

- They provide higher power.
- They can accommodate oversized NuBus cards.
- They support NuBus ’90 features.

Higher power

The power supply in the Macintosh Quadra 900 computer is designed to provide additional current on the +5-V outputs for the NuBus slots, compared with the current specified in *Designing Cards and Drivers for the Macintosh Family*, second edition. The Macintosh Quadra 900 has enough power to support a total of two 25-watt cards and three 15-watt cards.

Oversized NuBus cards

Each NuBus slot can accommodate either a standard NuBus card or an oversized card. The oversized card is the same length as a standard NuBus card, but it is 2 inches taller, as shown in Figure 2-2. Details A and B from Figure 2-2 are shown in Figure 2-3. Each NuBus slot in the Macintosh Quadra 900 computer includes a card guide; to install an oversized card, the user removes the card guide. You cannot install an oversized NuBus card in any other Macintosh II–family computer.

- **Figure 2-2** Dimensions of oversized card for NuBus

- **Figure 2-3** Detail dimensions of an oversized card for NuBus

NuBus ’90 features

NuBus ’90 is the 1990 proposal for revision of the IEEE standard for the NuBus (IEEE Std. R1196-R-1990). The NuBus slots in the Macintosh Quadra 900 computer provide the following new features described in that proposal:

- Low current at +5 V is available on the new STDBYPWR pin when main power is off and the AC cord is plugged in.
- New signals /TM2, /CLK2X, and /CLK2XEN support block transfers at double the standard rate. The Macintosh Quadra 900 computer allows double-rate block transfers between NuBus cards but does not support double-rate transfers to or from the main memory.
- NuBus ’90 defines new signals SB0 and SB1 for a serial bus on the formerly reserved pins A2 and C2. The serial-bus signals are bused and terminated, but the main circuit board does not drive them.

- NuBus ’90 defines new signals /CM0, /CM1, /CM2, and /CBUSY to support a cache- coherency protocol. Pins on the NuBus connector are assigned to those signals, but the Macintosh Quadra 900 system doesn’t support them.

Table 2-1 lists the new signals described in the proposal for NuBus ’90.

- **Table 2-1** NuBus '90 signals on the Macintosh Quadra 900 NuBus connector

Pin number	Signal name	Function
A2	SB0†	High-speed serial bus, defined in NuBus '90 proposal.
B8	/TM2†	New transfer mode: requests double-speed transfer.
B9	/CM0†	For cache-coherency operations.
B10	/CM1†	For cache-coherency operations.
B11	/CM2†	For cache-coherency operations.
B24	/CLK2X	Synchronizes double-speed block transfers.
B25	STDBYPWR	Small current at +5
B26	/CLK2XEN	If not connected to other NuBus '90 signals, enables /CLK2X driver.
B27	/CBUSY†	Used with cache-coherency operations.
C2	SB1†	High-speed serial bus, defined in NuBus '90 proposal.

†These signals are not driven or monitored by circuits in the Macintosh Quadra 900 computer.

♦ **Important** The eight lines that were connected to the –5.2-V supply in the original NuBus specification are now used for new features. Many older NuBus cards connect those eight lines together; the presence of such a card in a Macintosh Quadra 900 computer will disable the new features that use those lines. All other features of both old and new cards will operate normally. ♦For a complete listing of the NuBus connector pin assignments (not including the new NuBus '90 signals) and a description of the signals, see Chapter 5, "NuBus Card Electrical Design Guide," in *Designing Cards and Drivers for the Macintosh Family.*

Processor-direct slot

For maximum performance, the processor-direct slot (PDS) is connected directly to the MC68040 microprocessor by way of the system bus. (For a description of the system bus, see the section "Design Architecture" in Chapter 1.)

A PDS card for the Macintosh Quadra 900 computer has the same dimensions as a NuBus card and can include a back-panel connector. When the PDS card is installed, it occupies NuBus slot $E, reducing the number of available NuBus slots from five to four.

Possible applications for a PDS expansion card include cache memory, a video frame buffer, a DMA-based I/O controller, expansion memory, or even an additional MC68040 microprocessor.

- *Note:* The ROM software in the Macintosh Quadra 900 computer may not support those hypothetical PDS cards.

PDS card specifications

The PDS connector is a 140-pin connector manufactured by KEL Connectors, Incorporated. The connector on the main circuit board is KEL part number 8817-140-170SH; the corresponding connector on the PDS card is part number 8807-140-170LH.

Figure 2-4 shows the locations of both the PDS connector and the NuBus connector on the PDS card. Normally only the PDS connector is present on a PDS card.

Table 2-2 lists the signals on the pins of the PDS connector. Most of those signals are connected directly to pins on the MC68040 microprocessor. Table 2-3 defines the PDS signals that are not directly connected to the microprocessor. Table 2-4 shows two PDS signals that are connected to the microprocessor but that are not to be connected to a microprocessor on a PDS card.

- **Figure 2-4** Dimensions of the PDS card

• **Table 2-2** Pinouts of the PDS connector

Pin number	Signal name	Pin number	Signal name
1	GND	36	D4
2	A1	37	+5V
3	A3	38	D1
4	A4	39	GND
5	A6	40	SIZ1
6	A7	41	R/W
7	A9	42	/TIP.CPU
8	A11	43	n.c.
9	A13	44	/TEA
10	A15	45	/DLE
11	GND	46	SC1
12	A18	47	/TRST
13	A19	48	/CIOUT
14	A21	49	GND
15	A23	50	/BR.CPU
16	A24	51	/BR.40SLOT
17	A26	52	/BB
18	A29	53	/LOCK
19	A31	54	/MEMRESET
20	D31	55	/RSTO
21	D29	56	+5V
22	D27	57	n.c.
23	D25	58	/NMRQ6
24	D24	59	GND
25	D22	60	/IPL0
26	+5V	61	/IPL1
27	D19	62	/IPL2
28	D17	63	–12V
29	GND	64	GND
30	D14	65	n.c.
31	D13	66	n.c.
32	D11	67	n.c.
33	D9	68	n.c.
34	D8	69	n.c.
35	D6	70	+5V

(continued)

• **Table 2-2** Pinouts of PDS connector (continued)

Pin number	Signal name	Pin number	Signal name
71	AUX.CPUCLK	106	D5
72	A0	107	D3
73	A2	108	D2
74	+5V	109	D0
75	A5	110	SIZ0
76	GND	111	+5V
77	A8	112	/TBI
78	A10	113	/TA
79	A12	114	GND
80	A14	115	/TS
81	A16	116	SC0
82	A17	117	/MI
83	+5V	118	/MI.SLOT
84	A20	119	/BG.40SLOT
85	A22	120	/BG.CPU
86	GND	121	+5V
87	A25	122	TT0
88	A27	123	TT1
89	A28	124	GND
90	A30	125	TLN0
91	D30	126	TLN1
92	D28	127	/ANALOGRESET
93	D26	128	TM0
94	GND	129	TM1
95	D23	130	TM2
96	D21	131	+5V
97	D20	132	/PDS.SLOT.E.EN
98	D18	133	+12V
99	D16	134	n.c.
100	D15	135	TCK
101	+5V	136	TMS
102	D12	137	n.c.
103	D10	138	n.c.
104	GND	139	n.c.

105	D7	140	+5V

♦ **Important** The signals on the PDS connector are connected directly to the MC68040 with no buffers. Therefore, the address, data, and AUX.CPUCLK lines on a PDS card must present capacitive loads of not more than 40 pF. All other lines must present capacitive loads of not more than 20 pF. ♦

♦ *Note:* The AUX.CPUCLK line is terminated with a series resistor. To reduce reflections on this line, all loads on the card should be lumped.

• **Table 2-3** Nonmicroprocessor signals on the PDS connector

Signal name	Direction*	Function
/ANALOGRESET	O	Open-collector line;
AUX.CPUCLK	O	Buffered version of main processor's bus clock
/BG.40SLOT	O	Bus grant for PDS card
/BR.40SLOT	I	Bus request for PDS card
/MEMRESET	O	Fast reset generated by JDB IC for Memory Control Unit IC
/MI.SLOT	I	Memory inhibit from PDS card to Memory Control Unit IC
/NMRQ6	I	NuBus slot $E interrupt; also connected to NuBus slot $E
/PDS.SLOT.E.EN	I	Notifies YANCC NuBus controller IC that PDS card is installed and is using memory space assigned to NuBus slot $E

*I indicates input from PDS card to main logic board; O indicates output from main logic board to PDS card.

- **Table 2-4** Restricted microprocessor signals on the PDS connector

Signal name	Direction*	Function
/IPL(0–2)	O	Interrupt priority lines from PAL; not to be used as wire-OR lines; can be monitored by PDS card.
/TIP.CPU	O	From MC68040 on main circuit board; not connected to any other part of computer.

*O indicates output from main logic board (but not necessarily the processor) to PDS card.

PDS signal load/drive limits

Table 2-5 shows the load presented or drive available to each pin of a Macintosh Quadra 900 PDS expansion card and indicates whether the signals are inputs or outputs. Using the signal /BB (Bus Busy) as an example, the column in Table 2-5, labeled "Load or drive limits" is interpreted as follows.

/BB is shown presenting a load of 100 µA/4 mA, 70 pF. This is the maximum expected load that an expansion card must drive when sending the /BB signal to the main logic board. The DC load is in the format *signal high/signal low*. This means that the expansion card must drive a load of up to 100 µA when it drives /BB high and a load of up to 4 mA when it drives /BB low. The AC load is given as 70 pF, the maximum capacitance to ground presented by the main logic board to AC signals from the expansion card.

/BB is shown presenting a drive of 40 µA/.4 mA, 20 pF. This is the maximum amount of drive from the main logic board that is available to integrated circuits on the expansion card. /BB can drive an expansion card DC load of up to 40 µA in the high state or up to .4 mA in the low state. The AC drive is given as 20 pF, the maximum capacitance to ground that an expansion card may present to AC signals on the /BB line.

- **Table 2-5** 68040 Direct Slot signals, loading or driving limits

Signal name	Input/output	Load or drive limits
A0–A31	Input/output	Load: 200 µA/2 mA, 150 pF Drive: 40 µA/.4 mA, 40 pF
/ANALOGRESET	Output	Drive: 40 µA/.4 mA, 20 pF
AUX.CPUCLK	Output	Drive: 40 µA/.4 mA, 40 pF
/BB	Input/output	Load: 100 µA/4 mA, 70 pF Drive: 40 µA/.4 mA, 20 pF
/BG.CPU	Output	Drive: 40 µA/.4 mA, 20 pF
/BG.40SLOT	Output	Drive: 40 µA/.4 mA, 20 pF
/BR.CPU	Input	Load: 100 µA/4 mA, 40 pF
/BR.40SLOT	Input	Load: 100 µA/4 mA, 40 pF
/CIOUT	Output	Drive: 40 µA/.4 mA, 20 pF
D0–D31	Input/output	Load: 200 µA/2 mA, 120 pF Drive: 40 µA/.4 mA, 40 pF
/DLE	Input	Load: 100 µA/4 mA, 25 pF
/IPL0–/IPL2	Output	Drive: 40 µA/.4 mA, 20 pF
/LOCK	Input/output	Load: 100 µA/4 mA, 25 pF Drive: 40 µA/.4 mA, 20 pF
/MEMRESET	Output	Drive: 40 µA/.4 mA, 20 pF
/MI	Input/output	Load: 100 µA/4 mA, 25 pF Drive: 40 µA/.4 mA, 40 pF
/MI.SLOT	Input	Load: 100 µA/4 mA, 20 pF
/NMRQ6	Input	Load: 100 µA/4 mA, 40 pF
/PDS.SLOT.E.EN	Input	Load: 100 µA/4 mA, 20 pF
R/W	Input/output	Load: 100 µA/4 mA, 100 pF Drive: 40 µA/.4 mA, 20 pF
/RSTO	Output	Drive: 40 µA/.4 mA, 20 pF
SC0-SC1	Input/output	Load: 100 µA/4 mA, 40 pF Drive: 40 µA/.4 mA, 20 pF
SIZ0–SIZ1	Input/output	Load: 100 µA/4 mA, 90 pF Drive: 40 µA/.4 mA, 20 pF
/TA	Input/output	Load: 100 µA/4 mA, 100 pF Drive: 40 µA/.4 mA, 20 pF
/TBI	Input/output	Load: 100 µA/4 mA, 100 pF Drive: 40 µA/.4 mA, 20 pF

(continued)

• **Table 2-5** 68040 Direct Slot signals, loading or driving limits (continued)

Signal name	Input/output	Load or drive limits
TCK	Input	Load: 100 µA/4 mA, 25 pF
/TEA	Input/output	Load: 100 µA/4 mA, 100 pF Drive: 40 µA/.4 mA, 20 pF
/TIP.CPU	Output	Drive: 40 µA/.4 mA, 20 pF
TLN0–TLN1	Output	Drive: 40 µA/.4 mA, 20 pF
TM0–TM2	Output	Drive: 40 µA/.4 mA, 20 pF
TMS	Input	Load: 100 µA/4 mA, 25 pF
/TRST	Input	Load: 100 µA/4 mA, 25 pF
/TS	Input/output	Load: 100 µA/4 mA, 90 pF Drive: 40 µA/.4 mA, 20 pF
TT0–TT1	Input/output	Load: 100 µA/4 mA, 90 pF Drive: 40 µA/.4 mA, 20 pF

♦ *Note:* Input denotes direction from PDS card to main logic board, but not necessarily the processor. Output denotes direction from main logic board, but not necessarily the processor, to the PDS card.

PDS card design considerations

A PDS card can have memory locations in the upper part of the RAM memory space or in the space assigned to NuBus slot $E. (See the NuBus memory map in Figure 1-3 of Chapter 1, “The Macintosh Quadra 900 Hardware.”) If the card uses slot $E addresses, it must decode all addresses in both the slot space and the superslot space, responding to any access to an unused location with a /TEA (Transfer Error Acknowledge) on the processor bus to indicate an illegal address.

A typical PDS card maps into the NuBus space and works with the system software’s Slot Manager. Such a card must contain a NuBus declaration ROM and must notify the NuBus controller that it is using the NuBus space by asserting (pulling low) the signal /PDS.SLOT.E.EN on the PDS connector.

A PDS card that asserts the /PDS.SLOT.E.EN signal must issue a /TA (Transfer Acknowledge) or a /TEA in response to all accesses to the $E*xxx xxx* and $FE*xx xxxx* address space. (This action will keep the machine from hanging, since there is no timeout timer for slot $E when the /PDS.SLOT.E.EN signal is asserted.)

A PDS card functioning as bus master must must drive all control signals to a known state when it requests the system bus. Snoop control bits, in particular, must be driven to indicate no snoop.

By convention, all devices on the system bus, including a PDS card, must drive tristate signals active for one-half of a clock cycle before going tristate. For example, a PDS card functioning as the slave should drive /TA high after the address space is decoded, then drive it low for one clock cycle, and finally drive it high at the end of that clock cycle.
/TA should go tristate one-half clock cycle later. If you follow these guidelines in your PDS card design, the control lines will have cleaner edges, resulting in more reliable operation of your card.

♦ **Warning** A PDS expansion card for the Macintosh Quadra 700 computer must be designed to work with the MC68040 microprocessor; PDS cards designed for computers that use the MC68020 or the MC68030 will not work in the Macintosh Quadra 900 computer. ♦

Timing considerations

The signal timing for the PDS connector depends on the clock speed of the 68040 microprocessor. Developers of PDS expansion cards should clearly indicate on the card the maximum clock speed of the card.

The timing of a PDS card's output signals must be equal to or better than the worst-case delay output timing of the 68040 microprocessor. Also, input signals to a PDS card
cannot expect more setup time than is required for a signal to set up on the
68040 microprocessor.

Macintosh Quadra 900 Direct Slot interrupt handling

The interrupt-handling mechanism for the 68040 Direct Slot on the the Macintosh Quadra 900 is similar to the one used in the Macintosh II family. The five NuBus interrupt signals (Slot E is shared by the 68040 Direct Slot), the built-in video interrupt signal, and the Ethernet controller interrupt signal are routed through an OR gate to generate a signal
called /SLOTIRQ. This signal is connected to the CA1 input of VIA2, the second VIA chip
on the logic board. This VIA generates a level 2 interrupt to the MC68040. This VIA can
also generate an interrupt in response to SCSI requests, sound chip requests, or
VIA timer requests.

All interrupts to the MC68040 are autovectored. When the MC68040 is executing a level *x* interrupt, it first sets the interrupt mask to level *x*, so further interrupts at level *x* and below will be ignored. Once the interrupt handler is executed and an RTE instruction is processed, the interrupt mask is restored to the value it had before the interrupt.

The first-level interrupt dispatcher determines which hardware device—SCSI, sound chip, real-time clock, or expansion slot—is requesting the interrupt and dispatches code to the appropriate interrupt handler. If the interrupt generated by the VIA is a slot interrupt, the software polls the second VIA, bits PA0 through PA6, to determine which slot generated the interrupt. Table 2-6 summarizes the interrupt lines for VIA2.

- **Table 2-6** VIA2 interrupt lines

Address	Description
PA0	Ethernet IRQ
PA1	Slot $A IRQ
PA2	Slot $B IRQ
PA3	Slot $C IRQ
PA4	Slot $D IRQ
PA5	Slot $E IRQ
PA6	Video IRQ

Once the software determines which pseudoslot generated the interrupt, the Slot Manager software executes the interrupt handler for that slot device. The handler for that device was installed at boot time, when the initialization software polled the possible slots and identified the existence of a card in the slot by its ROM signature.

There is a delay between the assertion of a slot interrupt and the actual execution of the interrupt handler. During this time, the software polls the actual slot /IRQ signal. The recommended design practice is to latch the slot /IRQ signal so that once it is asserted, the interrupt handler software for the card has the responsibility of clearing the interrupt. This ensures that the slot /IRQ signal is asserted when polled and that the Slot Manager is dispatched correctly.

In addition to the standard Macintosh II functions, the VIA1 includes two new bits. The first is a software interrupt signal, and the second is the A/UX interrupt enable signal. When the software interrupt bit is set, an interrupt will be passed to the MC68040. When the A/UX interrupt enable bit is set, the interrupt control PAL will remap the interrupts. Table 2-7 shows the Macintosh and A/UX operating system interrupts, where priority 0 is low, and priority 7 is high.

- **Table 2-7** Interrupt mapping

Interrupt priority	Macintosh interrupt	A/UX interrupt
0		
1	VIA1	Software
2	VIA2 (SCSI, sound, NuBus slots, Ethernet, video)	VIA2 (SCSI, NuBus slots, video)
3		Ethernet
4	SCC	SCC
5		Sound
6		VIA1
7	NMI/YANCC err	NMI/YANCC err

Chapter 3 **ROM Features**

This chapter describes the ROM software in the Macintosh Quadra 900 computer, with emphasis on the new features.

The Macintosh Quadra 900 ROM uses a1 MB ROM in a Macintosh computer. The first half of the ROM is an overpatch of the 512 KB ROM used in other members of the Macintosh-II family. The second half of the ROM is new software to support the new features of the Macintosh Quadra 900 computer. “ROM Memory Map” at the end of this chapter describes the format of the ROM.

The Macintosh Quadra 900 ROM includes new code in several areas, including

- support for the MC68040, including FPU, MMU, and caches
- support for video hardware
- support for new custom ICs
- new software enhancements

ROM support for the MC68040

The MC68040 microprocessor is different in many ways from the MC68030 and earlier members of the 68000 family. The MC68040 incorporates a built-in floating-point unit (FPU), a built-in memory management unit (MMU), caches for instructions and data, and many other new features that contribute to its improved performance. The ROM for the Macintosh Quadra 900 computer incorporates the many changes required to take advantage of the new features of the MC68040.

Support for built-in FPU

The ROM software for the Macintosh Quadra 900 computer includes new code to support the differences between the floating-point unit in the MC68040 and the MC68881 and MC68882 FPUs used with the MC68020 and MC68030.

The method of detecting an FPU that was used in earlier ROM software does not work for the FPU in the MC68040, so the new ROM uses a different method. Also, the floating-point software in the new ROM incorporates several enhancements to the SANE routines, including ΩSANE, which speeds up SANE calls made by way of A-traps.

The FPU in the MC68040 does not handle all the instructions and data types that the MC68881 and MC68882 handle, so the ROM software includes new code to deal with those instructions and data types. For example, the exception vector table has a new exception vector to software that handles data types not supported by the FPU.

Support for built-in MMU

The MMU in the MC68040 is different in many ways from the MC68851 used with the MC68020 and from the built-in MMU in the MC68030. The registers and table-entry layouts are different; also, the MC68040 does not support certain features of the MC68851 and the MMU in the MC68030. The new ROM software generates the correct tables and register values for either type of MMU.

- *Note:* The MMU opcodes on the MC68040 are different from those on the MC68030. For example, both microprocessors have a PTEST operation, but the PTEST opcode for the MC68030 generates an unimplemented-instruction exception on the MC68040.

The MMU is set up to support only one ROM address space and one I/O address space. Actually, only one address space for each is necessary, and mapping one image of each address space reduces the size of the MMU tables.

The Macintosh Quadra 900 computer and the Macintosh Quadra 700 computer are the first Macintosh models to combine an MMU with built-in video using frame buffers in separate banks of VRAM. The ROM software manages the address space for the video frame buffers separately from main memory.

Gestalt and SysEnvirons values

Applications can determine in which Macintosh model they are running in by using the Gestalt routine. Use the SysEnvirons routine on models that don't have the Gestalt routine. For the Macintosh Quadra 900 computer, the machine type for Gestalt is 20; the SysEnvirons machine type is 18. The Gestalt routine also returns some other useful values:

- In the processor field, env68040 = 5.
- The gestaltFPUType selector returns gestalt68040FPU = 3.
- The gestaltMMUType selector returns gestalt68040MMU = 4.
- The gestaltProcessorType selector returns gestalt68040 = 5.

Support for new CopyBack cache mode

The MC68040 microprocessor has two internal caches, one for instructions and one for data. The caches perform the same function as those on earlier processors, storing the contents of recently addressed memory locations in anticipation that those contents will soon be used again.

The data cache in the MC68040 microprocessor has a new mode called the CopyBack mode. That mode is different from the WriteThru mode used by the caches in the MC68020 and MC68030 microprocessors. The CopyBack mode improves the overall performance because the processor may write to a memory location several times before the data must be flushed from the cache. Operating in the CopyBack mode can increase the processor's performance by up to 50 percent but also requires the operating system to manage some types of data more carefully.

The difference between the WriteThru and CopyBack modes on the MC68040 is the way they deal with data being written to memory. In WriteThru mode, the MC68040 writes the data to main memory immediately and also updates the cache. In CopyBack mode, the MC68040 writes directly to the cache, and main memory is not immediately updated. The cache then writes the data to main memory when that portion of the data cache is selected for replacement or when the data cache is flushed.

Cache management by the ROM

One consequence of the use of CopyBack mode is that main memory does not always contain the latest data. One way that old data can cause a problem is when an alternate bus master reads from memory that is being cached by the main processor and has not been updated. To prevent this problem from arising, the ROM software uses only pages marked uncacheable when setting up communication areas with alternate bus masters.

Another way old data can cause a problem is when the microprocessor fills its instruction cache from an area with old data. To prevent that problem, the ROM software flushes the contents of the data cache to main memory after writing data that consists of instruction code. Specifically, the software flushes the data cache to main memory after each of the following operations:

- loading a resource into memory
- moving a heap block
- creating a jump table

♦ *Note:* The ROM software in the Macintosh Quadra 900 computer invalidates the caches in the MC68040 microprocessor in the same places that the older ROM software invalidated the caches in the MC68020 and MC68030 microprocessors.

Cache management by applications

It has always been important to flush the caches on the MC68020 and MC68030 before executing instructions that were recently written to memory. On the MC68040, flushing only the instruction cache in this situation is not sufficient. The instruction and data caches are independent of each other, and there is a strong possibility that the instruction cache will fill with old data from RAM while the new data has not yet been written to RAM from the data cache.

To prevent this problem in your applications, it is vital that you use one or more of the calls provided by the system software whenever you write data that will be executed as instructions. Macintosh Technical Note 261 documents the _FlushInstructionCache and _FlushDataCache calls, which allow you to flush the caches. Because the purpose of the _FlushInstructionCache call is to maintain cache coherency, its operation on the MC68040 is to flush both the instruction and data caches. Flushing both caches with one call also avoids problems in situations where interrupts might occur while the caches are being flushed individually.

♦ **Important** Flushing the cache at certain times is critically important, but it is also important not to flush the cache too often. Unnecessary flushing of the cache impairs the performance of the MC68040 microprocessor. ♦

New exception handlers

Unlike the previous processors in the 68000 family, the MC68040 handles exceptions by the method called instruction restart. The processor recognizes exceptions at each instruction boundary in the execute stage of the integer pipeline and forces later instructions that have not yet reached the execute stage to be aborted. Also, the MC68040 creates some new exception stack frames, including those for its version of bus errors, which are called access errors.

Exception handlers, particularly bus error handlers, are affected by those differences. The ROM software includes appropriate changes to the universal startup code and modified bus error handlers for the Slot Manager and the Memory Manager.

ROM support for the video hardware

The Macintosh Quadra 900 computer has built-in video hardware with dedicated VRAM frame buffers controlled by a new custom IC called DAFB. The ROM software includes a new video driver to support the new hardware.

Because the MC68040 puts data on the data bus in a way that is different from the way the MC68020 and MC68030 do, the software on Apple's older video display cards must be modified to function correctly with the MC68040. The ROM software in the Macintosh Quadra 900 computer patches the ROM software on the display cards so that they operate normally. The affected cards are the Macintosh II Video Card and early versions of Macintosh Display Cards 4•8 and 8•24.

The problem with the video cards occurs because the cards rely on a feature of the MC68020 and MC68030 called byte smearing that is absent from the MC68040. The Slot Manager and the Device Manager have been patched to recognize those cards and substitute corrected code for their primary initialization software and video driver.

♦ *Note:* Third-party accelerator cards that use the MC68040 will encounter the byte-smearing problem when used with the older display cards listed above. For more information, refer to Macintosh Technical Note 282.

ROM support for new ICs

The ROM software includes new routines to support the following new ICs:

- Sonic IC (National DP83932) for built-in Ethernet
- NCR 53C96 IC for SCSI ports
- Caboose IC for real-time clock and parameter RAM
- MCU IC for memory addressing and control
- Enhanced ASC, Sporty, and DFAC ICs for sound processing

Support for Sonic Ethernet controller

The ROM software includes a new driver to support the Sonic IC. Developers can contact Apple Evangelism to obtain more information about built-in Ethernet, FriendlyNet, and Apple AUI.

Support for SCSI controllers

The ROM software supports the dual SCSI bus design using the NCR 53C96. Because the same ROM code will be used in future models that do not use those ICs, and because of the changes needed to support the dual SCSI bus, the ROM software that supports the SCSI Manager is a separate module addressed by a vector that is set up at startup time.

- *Note:* Even though there are two SCSI buses, there is only one set of SCSI ID numbers. That is, for compatibility with existing applications, the total number of SCSI devices is still only seven.

Support for Caboose real-time clock IC

In addition to providing the real-time clock and parameter RAM, the Caboose IC supports the new keyswitch feature on the Macintosh Quadra 900 computer. Operation of the keyswitch is described in Chapter 1, “The Macintosh Quadra 900 Hardware.”

The Caboose IC also provides a method of controlling the DFAC sound input IC. The ROM software sends the Caboose IC a message containing a string to be passed to the DFAC. The Start Manager sets the default values for the DFAC; the Sound Manager communicates with the DFAC by calling ROM routines.

Support for the MCU IC

Main RAM in the Macintosh Quadra 900 computer consists of four banks that begin on 64 MB boundaries. At startup time, the ROM software determines the amount of RAM installed in each bank and stores the actual bank sizes in registers in the MCU IC. Using those bank sizes, the MCU IC decodes bus addresses so that the separate physical banks of RAM occupy contiguous addresses in logical memory space.

Support for custom sound ICs

The ROM software for the Macintosh Quadra 900 computer supports the new Enhanced ASC, Sporty, and DFAC custom ICs. In addition to supporting the sound modes provided by the previous Apple Sound Chip, the new ICs and software support a record mode for sound input and sound playback from the internal CD-ROM.

ROM software enhancements

The ROM software includes the following enhancements:

- support for a RAM disk
- support for virtual memory (VM)
- an enhanced DebugUtil routine
- enhancements to QuickDraw
- an enhanced BlockMove routine

Support for RAM disk

The ROM software includes the capability to create a RAM disk that can then be used as the startup disk. The idea of a RAM disk was first proposed for the Macintosh Portable as a way of saving power by eliminating the need for continual disk activity. The RAM disk also increases performance of programs that execute and fetch data from the RAM disk, including the Macintosh Operating System.

In order for the RAM disk to work on a machine that uses an MMU, the RAM disk must be supported by ROM software. The software determines that the RAM disk is operating during warm starts and makes sure that its contents are not corrupted during the startup process.

The RAM disk driver works in concert with the MMU to protect the contents of the RAM disk from runaway applications. Using the MMU, the driver write-protects the memory pages that make up the RAM disk. The driver can unprotect individual pages when it is called upon to write data to disk, but the driver immediately protects the pages again before it exits. By protecting the contents of the RAM disk, the driver makes it possible for the user to restart the system from the RAM disk even after a system crash or reset.

Support for virtual memory

Starting with the Macintosh IIci computer, ROM software has provided some of the virtual memory (VM) routines to allow programmers to manipulate the tables in the MMU. The ROM software for the Macintosh Quadra 900 computer includes modifications to those routines to support the MC68040, along with some enhancements to provide write-protection capability for the main memory.

Specifically, the existing routines LockMemory, LockMemoryContiguous, and UnlockMemory can change the attributes of individual pages in the absence of VM. Also, two new calls, ProtectMemory and UnprotectMemory, have been added to allow programmers to protect pages of memory.

The ability to set the attributes of individual pages in memory becomes important with the advent of the large internal caches of the MC68040 and the common use of alternate bus masters. For example, when an area in memory is used as a communication buffer between the main processor and an alternate bus master, that area of memory must be marked uncacheable to maintain cache coherency after writes from the alternate bus master. On earlier machines that used the MC68020 and MC68030, it was acceptable to turn off the entire cache whenever any pages needed to be uncacheable, due to the small sizes of the caches on those processors and the limited number of bus masters. On a machine with an MC68040 and on-board bus masters, such a practice would result in an unacceptable degradation of performance.

Enhanced DebugUtil routine

DebugUtil is a routine that provides debuggers with low-level services that would otherwise require direct hardware manipulation by the debugger. Putting that kind of hardware-dependent code into the ROM relieves debuggers of some of the burden of supporting different hardware platforms.

Enhancements to QuickDraw

Two new features of the Macintosh Quadra 900 computer provide opportunities for optimization of QuickDraw operations. Those features are the faster operation of the video frame buffer and a new instruction in the MC68040.

The DAFB has different modes of operation of the frame buffer. QuickDraw on the Macintosh Quadra 900 computer simply sets the DAFB to its fastest mode of operation (per display and per bit depth) and performs all drawing operations in that mode.

The MC68040 has a new instruction, MOVE16, that speeds the unmodified copy operation. Even though this operation is not used with clipping, depth conversion, colorizing, stretching, or shrinking, it is used for many operations such as vertical scrolling, where it provides a significant speedup. To incorporate this enhancement, the ROM software modifies QuickDraw at startup time.

Enhanced BlockMove routine

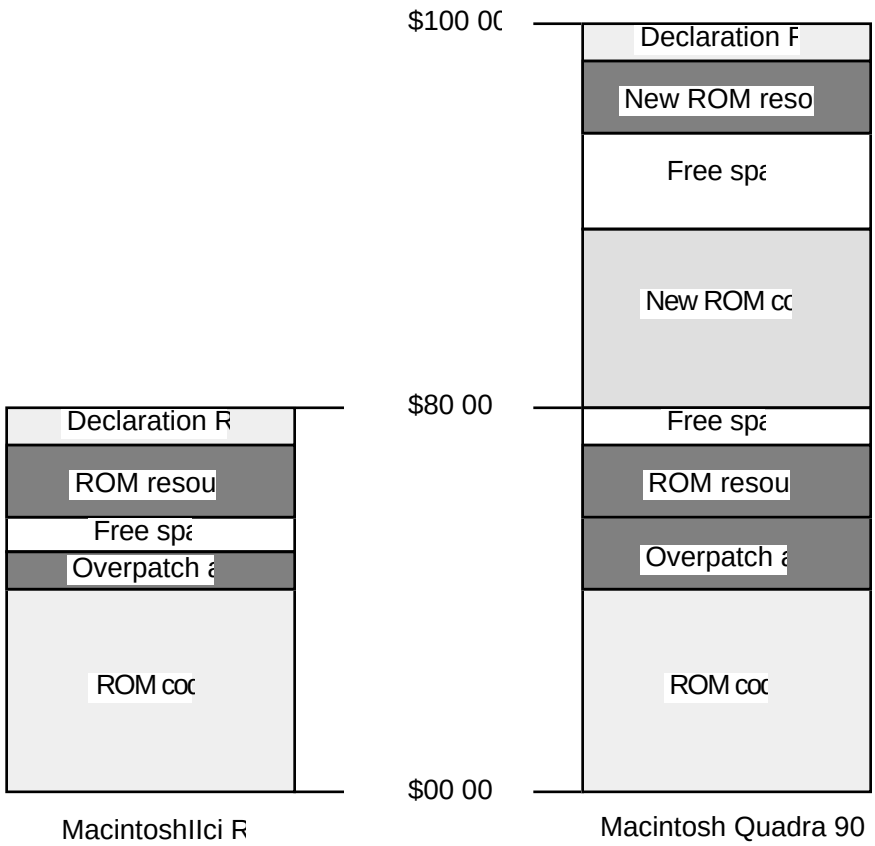
The BlockMove routine in the previous ROM software checks the length of all requested transfers and chooses from MOVE.B, MOVE.W, MOVE.L, and MOVEM.L instructions to move data from place to place in memory. The addition of the MOVE16 instruction in the MC68040 enables the new ROM software to provide further optimization.

ROM memory map

The ROM software for the Macintosh Quadra 900 computer is derived from the universal ROM used in the Macintosh IIci, Macintosh IIfx, Macintosh IIsi, and Macintosh LC computers. It uses the same patch file and supports all Macintosh models that use 32-bit processors—MC68020 and MC68030 as well as MC68040.

The Macintosh Quadra 900 ROM is the first 1 MB ROM used in a Macintosh computer. Figure 3-1 shows the memory map for the Macintosh Quadra 900 ROM along with the map for the earlier 512 KB ROM used in the Macintosh IIci, Macintosh IIfx, Macintosh IIsi, and Macintosh LC.

- **Figure 3-1** ROM memory maps



The first half of the ROM is an overpatch of the ROM used in the Macintosh IIci computer and preserves as much of the original ROM image as possible. The few changes include the startup diagnostics, located at the end of the code section, and the declaration ROM, which is always located at the highest addresses in the ROM.

The second half of the ROM contains the new code and resources needed to support the Macintosh Quadra 900 computer. The structure of the second half is similar to that of the first, with the code starting at low addresses and growing toward higher addresses, and the resources starting just below the declaration ROM and growing downward toward lower addresses. Because the ROM resources are stored in the form of a linked list, the resources in the second half of the ROM are available to the resource initialization code as simply a continuation of the original list of resources.

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