Developer Note

Macintosh IIvx

Also includes Macintosh IIvi and Performa 600

Developer Note

Developer Technical Publications

Apple Computer, Inc.
20525 Mariani Avenue
Cupertino, CA 95014
408-996-1010

Simultaneously published in the United States and Canada.

LIMITED WARRANTY ON MEDIA AND REPLACEMENT

If you discover physical defects in the manual or in the media on which a software product is distributed, APDA will replace the media or manual at no charge to you provided you return the item to be replaced with proof of purchase to APDA.

ALL IMPLIED WARRANTIES ON THIS MANUAL, INCLUDING IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, ARE LIMITED IN DURATION TO NINETY (90) DAYS FROM THE DATE OF THE ORIGINAL RETAIL PURCHASE OF THIS PRODUCT.

Even though Apple has reviewed this manual, APPLE MAKES NO WARRANTY OR REPRESENTATION, EITHER EXPRESS OR IMPLIED, WITH RESPECT TO THIS MANUAL, ITS QUALITY, ACCURACY, MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE. AS A RESULT, THIS MANUAL IS SOLD "AS IS," AND YOU, THE PURCHASER, ARE ASSUMING THE ENTIRE RISK AS TO ITS QUALITY AND ACCURACY.

IN NO EVENT WILL APPLE BE LIABLE FOR DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES RESULTING FROM ANY DEFECT OR INACCURACY IN THIS MANUAL, even if advised of the possibility of such damages.

THE WARRANTY AND REMEDIES SET FORTH ABOVE ARE EXCLUSIVE AND IN LIEU OF ALL OTHERS, ORAL OR WRITTEN, EXPRESS OR IMPLIED. No Apple dealer, agent, or employee is authorized to make any modification, extension, or addition to this warranty.

Some states do not allow the exclusion or limitation of implied warranties or liability for incidental or consequential damages, so the above limitation or exclusion may not apply to you. This warranty gives you specific legal rights, and you may also have other rights which vary from state to state.

Contents

Figures and Tables

About This Developer Note

This developer note describes the hardware and software features of the Macintosh IIvx computer. Two similar computers, the Macintosh IIvi and the Performa 600, are also discussed.

This document is written primarily for experienced Macintosh hardware and software developers who want to create products that are compatible with these new computers. If you are unfamiliar with Macintosh computers, or would simply like more technical information, you may want to read the related technical manuals listed in the following section.

Supplementary Documents

To supplement the information in this document, you might wish to obtain related documentation such as *Guide to the Macintosh Family Hardware*, second edition, *Designing Cards and Drivers for the Macintosh Family*, third edition, and *Inside Macintosh*. For detailed information about the Motorola 68030 microprocessor used in the Macintosh IIvx, refer to the *MC68030 Enhanced 32-Bit Microprocessor User's Manual*. For information about CD-ROM publishing, see the *Apple CD-ROM Handbook*. All of these books are available through APDA.

APDA is Apple's worldwide source for over 300 development tools, technical resources, training products, and information for anyone interested in developing applications on Apple platforms. To place an order or request a complimentary copy of the *APDA Tools Catalog*, contact

APDA
Apple Computer, Inc.
P.O. Box 319
Buffalo, NY 14207-0319

U.S.: 800-282-2732
Canada: 800-637-0029
International: 716-871-6555
FAX: 716-871-6511

AppleLink: APDA
America Online: APDA
CompuServe: 76666,2405
Internet: APDA@applelink.apple.com

Conventions and Abbreviations

This developer note uses abbreviations and typographical conventions that are standard in Apple publications.

Typographical Conventions

This note uses the following typographical conventions.

New terms appear in **boldface** where they are first defined.

Computer-language text—any text that is literally the same as it appears in computer input or output—appears in `Courier` font.

Standard Abbreviations

When unusual abbreviations appear in this book, the corresponding terms are also spelled out. Standard units of measure and other widely-used abbreviations are not spelled out.

Standard units of measure used in Apple reference books include:

A	amperes	MB	megabytes
GB	gigabytes	MHz	megahertz
Hz	hertz	ms	milliseconds
K	1024	ns	nanoseconds
KB	kilobytes	V	volts
mA	milliamperes	W	watts

Standard abbreviations used in Apple reference books include:

$*n*	hexadecimal value *n*
AC	alternating current
ADB	Apple Desktop Bus
CD-ROM	compact disc read-only memory
CLUT	color look-up table
DAC	digital-to-analog converter
IC	integrated circuit
ASIC	application-specific integrated circuit
MMU	memory-management unit
RAM	random-access memory
ROM	read-only memory

RGB	red-green-blue (a video display system used by Apple computers)
SCSI	small computer system interface
SVGA	super VGA (a video display system used with PC-type computers)
VGA	video graphics adapter (a video display system used with PC-type computers)
VRAM	video RAM

CHAPTER 1

Hardware

This chapter describes the major hardware features of the Macintosh IIvx computer, emphasizing the similarities and differences between this and other Macintosh computers. This chapter also provides information about two similar new models, the Macintosh IIvi and Performa 600, where they differ from the Macintosh IIvx. Unless otherwise noted, the features and specifications described in this developer note apply to all three computers.

The Macintosh IIvx is a new modular Macintosh computer offering features, performance, and expansion capabilities that make it an excellent choice for business, education, and multimedia users. The computer is housed in a sturdy metal enclosure slightly larger than that of the Macintosh IIci but with space available for a CD-ROM drive or other optional 5.25-inch half-height device.

Features

The Macintosh IIvx includes these features:

- Microprocessor: Motorola MC68030 running at 31.3344 MHz.
  - The Macintosh IIvi operates at 15.6672 MHz.
  - The Performa 600 operates at 31.3344 MHz.
- Floating Point Unit (FPU): Motorola MC68882 running at 31.3344 MHz.
  - An FPU is optional in the Macintosh IIvi and Performa 600. A socket is provided on the main logic board. The FPU operates at the same speed as the microprocessor.
- Read-only memory (ROM): 1 MB soldered to the main logic board.
- Random-access memory (RAM): 4 MB soldered to the main logic board. Four SIMM sockets for expansion up to 68 MB.
- RAM cache: 32 KB static RAM (SRAM) cache on the main logic board.
  - The Macintosh IIvi and Performa 600 do not include a RAM cache.
- Expansion: Three standard NuBus expansion slots. The power budget for NuBus cards is 13.9 watts each or 41.7 watts total.
- Accelerator slot: A Euro-DIN 120-pin connector on the main logic board facilitates system enhancements such as a faster microprocessor. The power budget for this slot is 5 watts (1000 mA at +5 volts).
- Floppy disk: One 1.4 MB Apple SuperDrive with SWIM (Super Woz Integrated Machine) interface.
- Hard disk: One internal 3.5-inch SCSI (Small Computer System Interface) hard disk is included in most configurations. Hard disk configurations range from 40 MB to 400 MB. As with all Macintosh computers, external SCSI hard disks are also supported.
- CD-ROM: One 5.25-inch SCSI CD-ROM drive is included in some configurations.
- I/O: Two Apple Desktop Bus (ADB) ports, two mini-DIN 8 serial ports, one SCSI port, one stereo headphone jack, one microphone jack, and one DB-15 video connector.

- Video: 16-bit color display capability on 640 x 480 RGB and VGA monitors.

  Standard configurations include 512 KB of video RAM (VRAM), allowing 16-bit color display on the the Apple 12-inch RGB monitor and 8-bit color on larger monitors. Some configurations include 1 MB of VRAM, providing 16-bit color on all supported monitors. Video memory can be increased from 512 KB to 1 MB using 100 ns VRAM SIMMs.

- Sound: Monaural sound input and output functionally identical to that of the Macintosh LC and LC II. Sound from an internal CD-ROM drive can be heard in mono through the built-in speaker or in stereo through the headphone jack. Users can record sounds with a microphone or directly from the CD-ROM drive.

- Networking: LocalTalk is standard. Ethernet is supported by optional Apple or third-party NuBus cards.

Table 1-1 highlights the differences between the Macintosh IIvx, the Macintosh IIvi, and the Performa 600.

Table 1-1 Comparison of the Macintosh IIvx, Macintosh IIvi, and Performa 600 computers

	Macintosh IIvx	**Macintosh IIvi**	**Performa 600**
Processor speed	32 MHz	16 MHz	32 MHz
RAM cache	32 KB	None	None
FPU	Standard	Optional	Optional

Compatibility Issues

This section identifies features of the Macintosh IIvx that developers should investigate to assure compatibility with their products.

RAM Cache

The Macintosh IIvx includes a 32 KB static RAM cache on the main logic board. While the cache circuitry in the Macintosh IIvx provides benefits similar to the Macintosh IIci cache card, there are a number of important differences in implementation. Most significantly, the Macintosh IIvx cache does not support snooping. Snooping allows multiple bus masters to maintain cache coherency without marking areas of memory non-cacheable. However, the Macintosh IIvx ROM software features improvements to the `LockMemory` and `LockMemoryContiguous` routines that allow non-cacheable communications areas to be allocated with little impact on system performance.

Bus master cards that write to shared memory locations must use the `LockMemory` and `LockMemoryContiguous` routines to identify non-cacheable memory. These routines are documented in *Inside Macintosh*. In general, applications that are compatible with Macintosh Quadra computers and with virtual memory under System 7 should be compatible with the Macintosh IIvx.

Accelerator Slot

The accelerator slot introduced in the Macintosh IIvx provides all the signals necessary to support an auxiliary microprocessor. This slot is similar to the Macintosh IIci cache slot, but does not include some of the cache control signals. Most of the signals on the accelerator slot are connected directly to the corresponding signals on the 68030.

▲ **WARNING**
The Macintosh IIvx accelerator slot is not compatible with processor-direct slot (PDS) cards designed for other Macintosh computers. Although the same 120-pin connector is used for the PDS on some Macintosh models, the electrical signals are different. Installing a PDS card in the Macintosh IIvx accelerator slot may damage both the computer and the card. ▲

SCSI Termination

An active termination circuit on the main logic board automatically terminates the internal SCSI bus when no external SCSI device is connected. If a terminated device is attached to the external SCSI port, the internal termination is deactivated, and the last device on the external bus must be terminated according to Apple SCSI specifications.

The active termination circuit eliminates the need for static termination of CD-ROM drives, hard disks, or other SCSI devices installed in the internal 5.25-inch device location. Developers must remove or disable terminators on internal 5.25-inch devices to ensure proper operation of the SCSI bus.

Note
A device installed in the internal 3.5-inch hard disk location must be terminated because it is the first device on the SCSI bus. ◆

Video Modes

The Macintosh IIvx does not support 1-bit video mode on the Apple 12-inch RGB monitor. Applications that require 1-bit mode may be incompatible with the Macintosh IIvx computer when this monitor is used. The Macintosh IIvx supports 1-bit mode on the 12-inch monochrome and 13-inch RGB monitors. To ensure that your applications work well with all types of monitors, use the appropriate QuickDraw routines to determine the resolution and video mode of the monitor attached to a Macintosh IIvx computer. These routines are documented in *Inside Macintosh*.

Floating Point Unit

Application software that takes advantage of an FPU must use the Gestalt Manager to determine if an FPU is installed in the Macintosh IIvi or Performa 600 computers. The Gestalt Manager is described in *Inside Macintosh*.

Because a mathematics coprocessor is not standard in all Macintosh models, application software should not expect or require an FPU. The Standard Apple Numerics Environment (SANE) package in the Macintosh Operating System automatically takes advantage of an FPU when available and provides optimized mathematics routines for use when an FPU is not present. SANE is described in the *Apple Numerics Manual*, second edition, available from APDA.

Hardware Overview

This section provides a functional description of the major hardware systems of the Macintosh IIvx computer. The block diagram in Figure 1-1 illustrates how the major components of the Macintosh IIvx are interconnected.

IMPORTANT

The memory sizes, addresses, and other information provided in this chapter are specific to the Macintosh IIvx, Macintosh IIvi, and Performa 600 computers and are provided for informational purposes only. To ensure that your application software is compatible with both current and future Macintosh systems you must use the Macintosh Toolbox and Operating System routines wherever provided. In particular, never use absolute addresses to access hardware, because these addresses are specific to a particular Macintosh model and are subject to change. ▲

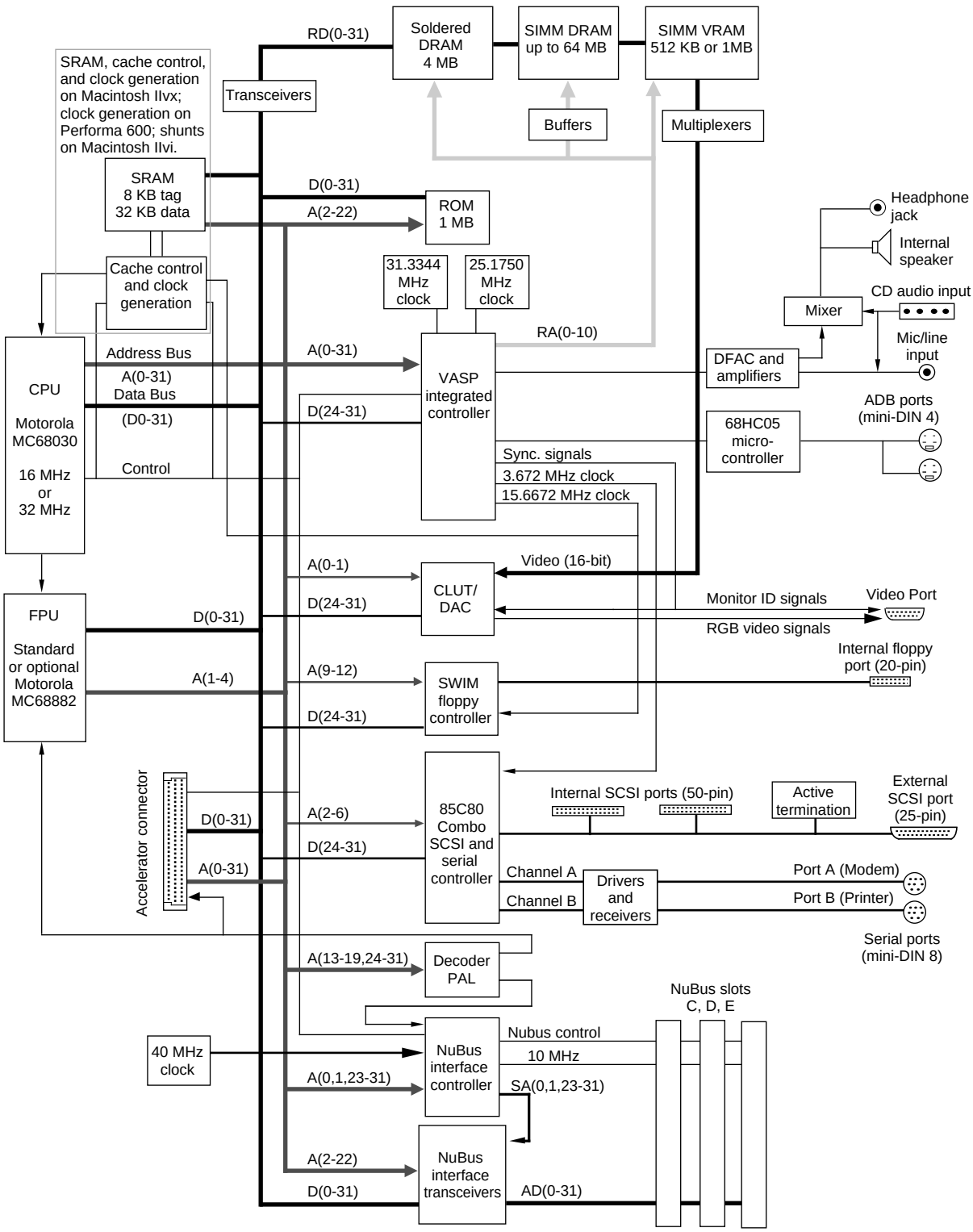
Main Processor

The Macintosh IIvx uses a 68030 microprocessor running at a clock rate of 31.3344 MHz. The microprocessor accesses RAM, ROM, and VRAM using 32-bit data transfers.

VASP Integrated Controller

The VASP integrated controller is a custom chip that implements many functions that were provided by individual chips in computers such as the Macintosh IIci. These functions include timing, video generation, memory mapping, sound, clock generation, and miscellaneous GLU (General Logic Unit) functions. The VASP chip is similar in many respects to the V8 gate array used in the Macintosh LC and LC II.

Figure 1-1 Block diagram of the Macintosh IIvx computer



Address Decode and Memory Mapping

Like other Macintosh computers that use the 68030 processor, the Macintosh IIvx supports both 24-bit and 32-bit memory addressing modes. The Macintosh IIvx hardware, however, always operates in 32-bit mode. The memory management unit (MMU) inside the 68030 works with the VASP's memory controller to map 24-bit addresses to their 32-bit equivalent. System or application software can select 24-bit addressing mode using the `SwapMMUMode` operating system routine described in *Inside Macintosh*.

In 32-bit mode, the 68030 processor supports a 4 GB address space. In 24-bit mode, however, the upper 8 address bits are ignored, and the maximum address space is limited to 16 MB. The VASP chip remaps address space so that RAM, ROM, VRAM, I/O, and expansion all appear in this 16 MB range. Although the address translation is transparent to software, it has the effect of limiting the amount of addressable RAM to 8 MB. Table 1-2 summarizes the 24- and 32-bit memory maps for the Macintosh IIvx.

IMPORTANT

The addresses shown in this section apply only to the Macintosh IIvx computer. It is highly recommended that you use the Macintosh Toolbox calls, system traps, and global variables listed in *Inside Macintosh* to access the hardware. ▲

Table 1-2 Macintosh IIvx memory map summary

Function	24-bit mode	32-bit mode
RAM	$00 0000–$7F FFFF	$0000 0000–$043F FFFF
ROM	$80 0000–$8F FFFF	$4000 0000–$403F FFFF
I/O space	$F0 0000–$FF FFFF	$50F0 0000–$50FF FFFF
VRAM	$B0 0000–$BF FFFF	$60B0 0000–$60BF FFFF
RAM disk	not addressable	$7000 0000–$743F FFFF
NuBus	$C0 0000–$EF FFFF	$8000 0000–$EFFF FFFF

Note

The VASP chip issues a bus error if you try to access address $FF FFFF in 24-bit mode or $FFFF FFFF in 32-bit mode. ◆

Video Generation

With the exception of the color look-up table (CLUT) and final output stage, the VASP chip provides all the video control circuitry for the Macintosh IIvx. The VASP chip senses the type of monitor attached to the video port, refreshes VRAM, controls access to the frame buffer, and controls all video timing signals.

Sound Control

The VASP's sound control circuitry is identical to that provided by the V8 gate array in the Macintosh LC and LC II, except that memory for the sound input and output buffers is located in VRAM rather than in DRAM.

GLU and VIA Functions

The VASP includes a full-function VIA1, a pseudo-VIA2 similar to that of the V8 gate array, and several registers similar to those of the Apple Sound Chip.

ROM

The Macintosh IIvx ROM is implemented as two 256K x 16-bit ICs providing 1 MB of read-only memory. In the Macintosh IIvx, a cache hit on a ROM read cycle is completed in 3 clock cycles, requiring no wait states. A cache miss requires 8 cycles, which is equivalent to 5 wait states at 32 MHz. ROM accesses always require 8 clock cycles in the Performa 600, which has no cache. The Macintosh IIvi requires 4 clock cycles for ROM accesses, which is equivalent to 1 wait state at 16 MHz.

Power-On Overlay Function

The Macintosh IIvx, like all other Macintosh computers, implements an overlay function at power-up or reset that maps ROM address space (in this case, $4000 0000 through $403F FFFF) to RAM space starting at location $0000 0000. Following the first access to the normal ROM address range, the ROM image at $0000 0000 is removed and replaced by RAM.

RAM

The Macintosh IIvx computer comes standard with 4 MB of RAM soldered to the main logic board. This memory consists of eight 1M x 4-bit dynamic RAM ICs, and occupies the address space from $0000 0000 through $003F FFFF.

Four SIMM sockets allow users to add up to 64 MB of additional RAM. The Macintosh IIvx uses the same 30-pin RAM SIMMs used in most other Macintosh models. SIMMs may be 256 KB, 1 MB, 2 MB, 4 MB, or 16 MB capacity, single or double sided. The Macintosh IIvx requires 80 ns or faster RAM. When adding additional RAM, all four sockets must be filled and all SIMMs must be the same size and speed.

Software determines the amount of RAM installed at system startup, and configures the system appropriately. Because RAM is tested and sized before the video system is initialized, the screen will appear blank during this phase of the boot process. Users with large amounts of RAM installed will experience a delay before the desktop pattern appears.

RAM read and write cycle timing is the same as the ROM read cycle timing described in the previous section. RAM writes require 8 clock cycles in the Macintosh IIvx because

the data is always written to main memory in addition to updating the cache. Burst transfers are not supported.

Video

The Macintosh IIvx video system is similar to that of the Macintosh LC and LC II, but provides support for 16-bit color on 640 x 480 RGB and VGA monitors. All video timing is controlled by the VASP chip. Video data is stored in a dedicated frame buffer provided by two VRAM SIMM modules.

VRAM access by the 68030 requires 4 clock cycles (1 wait state) in the Macintosh IIvi, and 8 clock cycles (5 wait states) in the Performa 600 and Macintosh IIvx.

Color modes up to 8 bits per pixel use a 256 x 24-bit CLUT which is provided by an enhanced version of the custom chip used in the LC and LC II. Monochrome modes also use the CLUT but drive the red, green, and blue inputs with the same signal. In 8-bit color mode applications can display as many as 256 colors from a palette of 16 million. The 16-bit color mode provides direct access to 32,768 colors.

VRAM

The Macintosh IIvx computer comes with 512 KB of VRAM provided by two 256 KB SIMMs. The Macintosh IIvx uses the same type of 68-pin VRAM SIMM as the Macintosh LC, LC II, and Macintosh Quadra computers. The Macintosh IIvx requires 100 ns or faster VRAM.

VRAM SIMMs must be installed in identical pairs. The two types of VRAM SIMMs that can be installed in the Macintosh IIvx are:

- 256 KB VRAM SIMM: These modules contain two 128K x 8-bit VRAMs. Two of these SIMMs provide a total of 512 KB VRAM. This is the standard configuration, and allows 16-bit color on 12-inch RGB monitors and 8-bit color on larger monitors.
- 512 KB VRAM SIMM: These modules contain four 256K x 4-bit VRAMs. Two of these SIMMs provide a total of 1 MB VRAM. This configuration allows users to display 16-bit color on 640 x 480 monitors.

The maximum addressable VRAM is 1 MB. VRAM SIMMs not listed above cannot be used in the Macintosh IIvx.

Developers should note that not all VRAM manufacturers meet Apple specifications. In particular, VRAM for the Macintosh IIvx, LC, and LC II must operate correctly with a DT/OE pulse width of 25 to 30 ns during read transfer cycles. VRAM requiring longer read transfer cycles may cause visible artifacts on the display.

Monitors Supported

Table 1-3 lists the monitors and video modes supported by the Macintosh IIvx computer's internal video circuitry. The monitor connects to the DB-15 external video connector and identifies itself by a hardwired 3-bit code. See *Guide to the Macintosh Family Hardware* for information about monitor identification codes.

Table 1-4 shows the pinout for the external video connector. If no monitor is detected, the Macintosh IIvx computer's video circuitry outputs setup and timing signals for the 12-inch RGB monitor.

Table 1-3 Macintosh IIvx video modes

Monitor	Resolution			Dot clock	VRAM
	Width (pixels)	Height (pixels)	Depth (bits)	(MHz)	
12-inch RGB	512	384	2	15.6672	Standard (512 KB)
	512	384	4	15.6672	Standard
	512	384	8	15.6672	Standard
	512	384	16	15.6672	Standard
13-inch RGB*	640	480	1	31.3344	Standard
	640	480	2	31.3344	Standard
	640	480	4	31.3344	Standard
	640	480	8	31.3344	Standard
	640	480	16	31.3344	1 MB
VGA	640	480	1	25.1750	Standard
	640	480	2	25.1750	Standard
	640	480	4	25.1750	Standard
	640	480	8	25.1750	Standard
	640	480	16	25.1750	1 MB

* Includes Macintosh Color Display, AppleColor High Resolution RGB Monitor, and Apple High Resolution Monochrome Monitor.

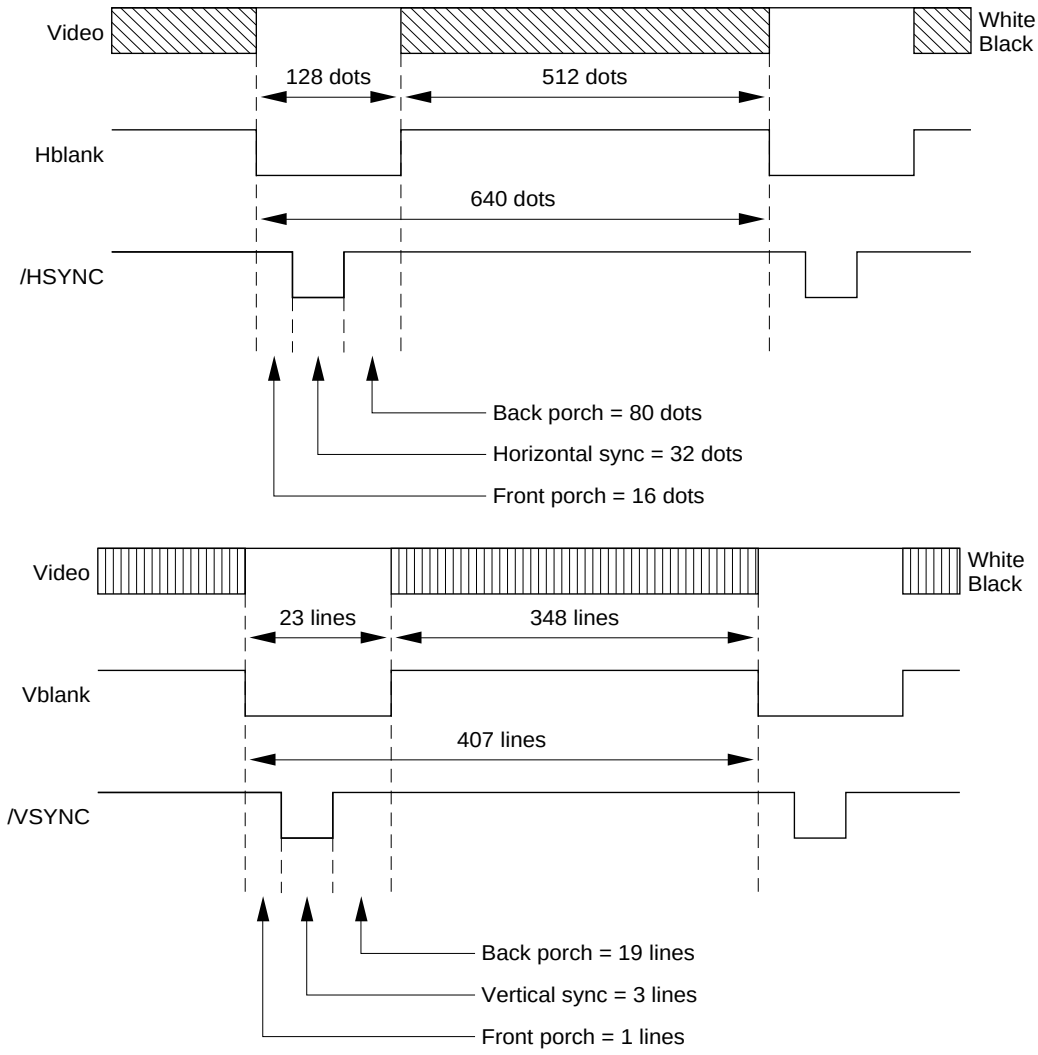
Table 1-4 External video connector pinout

Pin	Signal name	Description
1	RED.GND	Red video ground
2	RED.VID	Red video signal
3	/CSYNC	Composite synchronization signal
4	SENSE0	Monitor sense signal 0
5	GRN.VID	Green video signal
6	GRN.GND	Green video ground
7	SENSE1	Monitor sense signal 1
8	n.c.	Not connected
9	BLU.VID	Blue video signal
10	SENSE2	Monitor sense signal 2
11	GND	CSYNC and VSYNC ground
12	/VSYNC	Vertical synchronization signal
13	BLU.GND	Blue video ground
14	HSYNC.GND	HSYNC ground
15	/HSYNC	Horizontal synchronization signal
Shell	SGND	Shield ground

Video Timing

Figures 1-2, 1-3, and 1-4 show timing information for the supported video modes. The diagrams define the blanking, synchronizing, and active video regions of the video scan waveforms in terms of dot or pixel times. A dot is the time required to draw a single pixel.

Figure 1-2 512 x 384 video timing

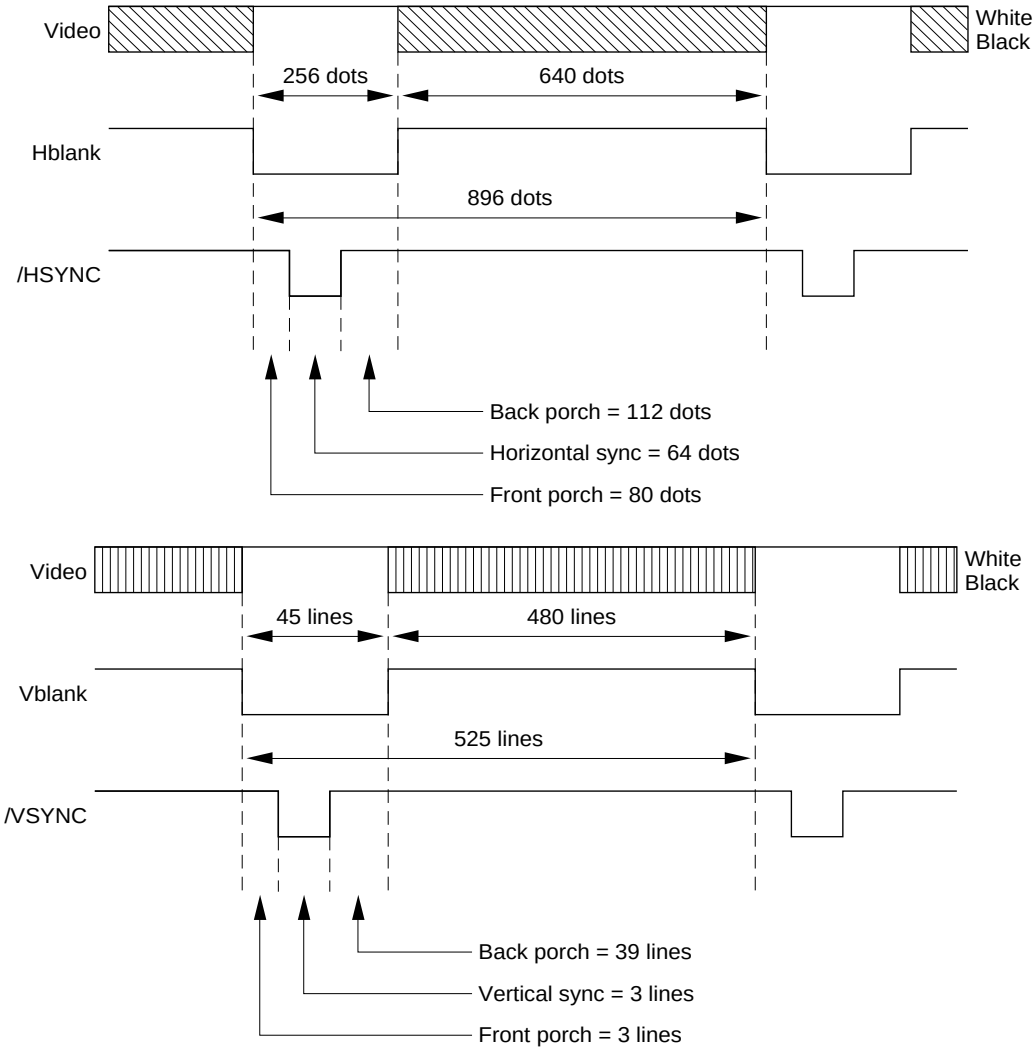


Dot clock = 15.6672 MHz
Dot = 63.83 ns

Full line = 40.85 µs
Line rate = 24.48 kHz

Full frame = 16.626 ms
Frame rate = 60.15 Hz

Figure 1-3 640 x 480 video timing

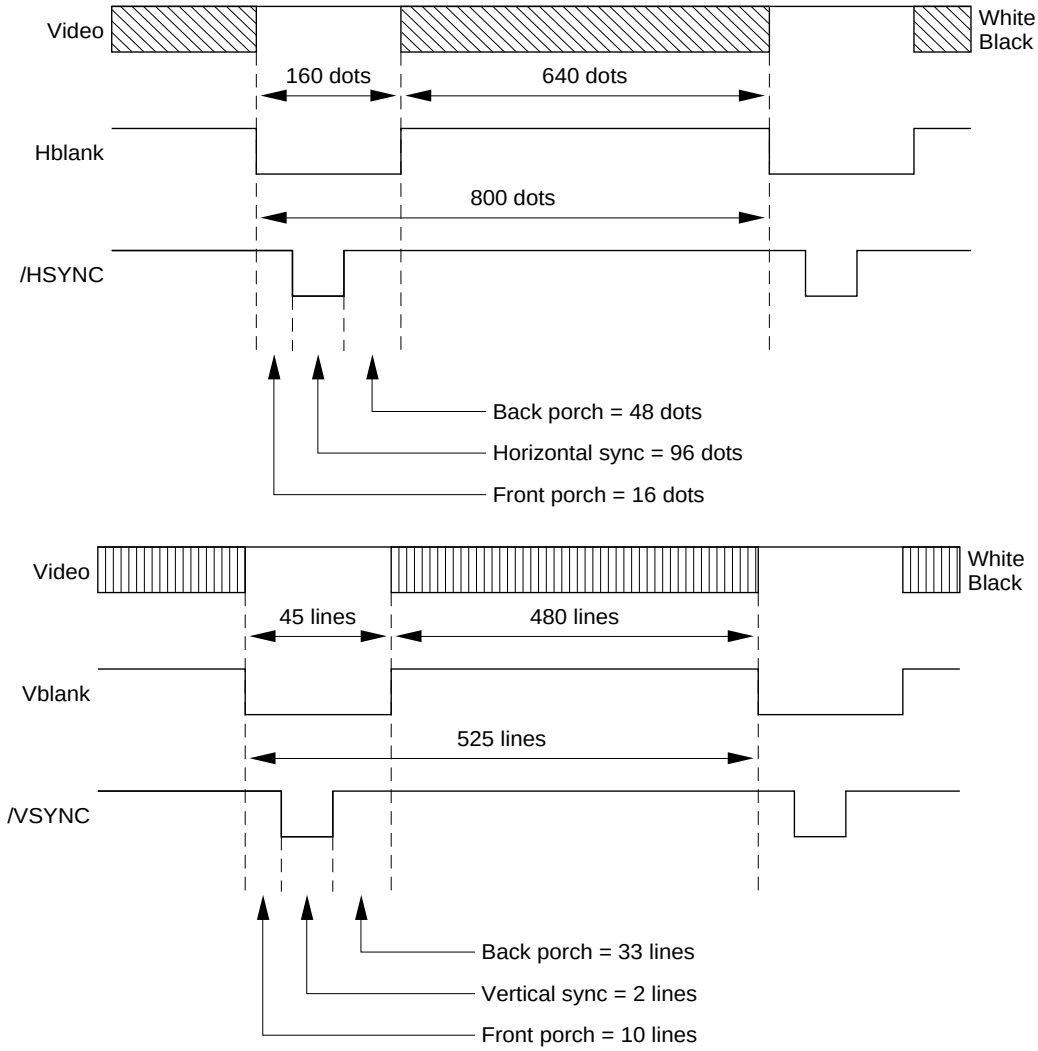


Dot clock = 31.3344 MHz
Dot = 31.91 ns

Full line = 28.59 µs
Line rate = 34.975 kHz

Full frame = 15.01 ms
Frame rate = 66.62 Hz

Figure 1-4 640 x 480 VGA timing



Dot clock = 25.175 MHz
Dot = 39.722 ns

Full line = 31.778 µs
Line rate = 31.469 kHz

Full frame = 16.68 ms
Frame rate = 59.94 Hz

Sound

The Macintosh IIvx sound system includes a built-in speaker, stereo headphone jack, microphone jack, and an internal CD audio input connector. Computer-generated sounds and CD audio are mixed and played in mono through the internal speaker. The headphone jack plays CD audio in stereo and computer-generated sounds in mono to both ears.

Users can record sounds with a microphone or directly from an internal CD-ROM drive. Plugging in a microphone overrides the CD audio input. An attenuator is required to record line-level audio through the microphone input.

The Macintosh IIvx sound hardware is essentially the same as that of the Macintosh LC and LC II, except that memory for the sound input and output buffers is located in VRAM rather than in DRAM. This change is transparent to application software that uses the Sound Manager.

Serial and SCSI Interfaces

The Combo serial communication and SCSI controller chip in the Macintosh IIvx combines the functions of the 85C30 serial communication controller (SCC) and 53C80 SCSI controller chips in a single device.

Serial Communication Controller

The SCC portion of the Combo chip provides two independent ports for serial communication. These ports are identical.

Two 8-pin miniature DIN connectors connect the SCC to the external world. The connectors are the same as those currently used on other Macintosh computers. Table 1-5 shows the pinout for the serial ports. Note that pin 7, which is used as a general purpose input in some Macintosh models, is not connected in the Macintosh IIvx.

Table 1-5 Serial port pinout

Pin number	Signal name	Signal description
1	HSKo	Handshake output
2	HSKi	Handshake input
3	TxD–	Transmit data –
4	GND	Ground
5	RxD–	Receive data –
6	TxD+	Transmit data +
7	n.c.	Not connected
8	RxD+	Receive data +

SCSI Controller

The SCSI controller in the Combo chip is completely compatible with the SCSI controller used on current members of the Macintosh family. It is designed to support the SCSI interface as defined by the American National Standards Institute (ANSI) X3T9.2 committee. The Macintosh IIvx includes two internal 50-pin SCSI connectors and one external DB-25 SCSI connector. These connectors are identical to those used on other members of the Macintosh family. Table 1-6 shows the pinouts for the SCSI connectors.

Table 1-6 Internal and external SCSI connector pinouts

Internal (50-pin)	External (25-pin)	Signal name	Signal description
2	8	/DB0	Bit 0 of SCSI data bus
4	21	/DB1	Bit 1 of SCSI data bus
6	22	/DB2	Bit 2 of SCSI data bus
8	10	/DB3	Bit 3 of SCSI data bus
10	23	/DB4	Bit 4 of SCSI data bus
12	11	/DB5	Bit 5 of SCSI data bus
14	12	/DB6	Bit 6 of SCSI data bus
16	13	/DB7	Bit 7 of SCSI data bus
18	20	/DBP	Parity bit for SCSI data bus
26	25	TPWR	+5 volts termination power
32	17	/ATN	Attention
36	6	/BSY	Busy
38	5	/ACK	Acknowledge
40	4	/RST	SCSI data bus reset
42	2	/MSG	Message
44	19	/SEL	Select
46	15	/C/D	Control/data
48	1	/REQ	Request
50	3	/I/O	Direction (input/output)
All odd pins (25 total)	7, 9, 14, 16, 18, and 24	GND	Ground

NOTE Pins not listed in Table 1-6 are not connected.

SCSI Termination

The SCSI bus must be terminated at both ends. Because the Macintosh IIvx may contain two internal SCSI devices, an active termination circuit automatically terminates the CD-ROM drive or other 5.25-inch device when it is the last device on the bus. If a terminated device is attached to the external SCSI port, the internal termination is deactivated.

The active termination circuit eliminates the need for static termination of CD-ROM drives, hard disks, or other SCSI devices installed in the internal 5.25-inch device location. Developers must remove or disable terminators on internal 5.25-inch devices to ensure proper operation of the SCSI bus.

Note
A device installed in the internal 3.5-inch hard disk location must be terminated because it is the first device on the SCSI bus. ◆

Floppy Disk Interface

The internal 3.5-inch Apple SuperDrive is controlled by the same SWIM chip used in other Macintosh computers. A 20-pin connector provides the signal interface between the SWIM chip and the drive. Table 1-7 shows the pinout for the floppy disk connector.

Table 1-7 Floppy disk connector pinout

Pin number	Signal name	Signal description
1	GND	Ground
2	PH0	Phase 0: state-control line
3	GND	Ground
4	PH1	Phase 1: state-control line
5	GND	Ground
6	PH2	Phase 2: state-control line
7	GND	Ground
8	PH3	Phase 3: register write strobe
9	n.c.	Not connected
10	/WRREQ	Write data request
11	+5V	+5 volts
12	SEL	Head select
13	+12V	+12 volts
14	/ENBL	Drive enable

continued

Table 1-7 Floppy disk connector pinout (continued)

Pin number	Signal name	Signal description
15	+12V	+12 volts
16	RD	Read data
17	+12V	+12 volts
18	WR	Write data
19	+12V	+12 volts
20	+5V	+5 volts

ADB Microcontroller

The Macintosh IIvx computer uses the same 68HC05 microcontroller first used in the Macintosh IIsi. The 68HC05 integrates the functions of the Apple Desktop Bus (ADB) controller, real-time clock (RTC), parameter RAM (PRAM), and power control.

ADB Interface

The ADB is a single-master, multiple-slave, serial communications bus that uses an asynchronous protocol and connects keyboards, graphics tablets, mouse devices, and other devices to the Macintosh IIvx computer. The custom ADB microcontroller drives the bus and reads status from the selected external device. A 4-pin mini-DIN connector connects the ADB controller to the outside world. Table 1-8 lists the ADB connector pinout.

Table 1-8 ADB connector pinout

Pin number	Signal name	Signal description
1	ADB	Bidirectional data bus used for input and output. An open-collector signal pulled up to +5 volts through a 470 ohm resistor on the main logic board.
2	PSW	Power-on signal.
3	+5V	+5 volts from the computer. A 1-amp fuse at the output satisfies safety requirements.
4	GND	Ground from the computer.

Real-Time Clock and Parameter RAM

The 68HC05 microcontroller provides RTC and PRAM functions for the Macintosh IIvx. When the computer is shut down, the 68HC05 is powered by the +5 V trickle output of the Macintosh IIvx power supply. That output provides power for the RTC, PRAM, and ADB power-on circuitry. A lithium backup battery allows the 68HC05 to maintain the clock and PRAM data when the computer is unplugged.

Low-level access to the RTC and PRAM is accomplished through modified ADB-style commands. Applications that use documented routines to read and write to the RTC and PRAM will work without modification on the Macintosh IIvx.

Soft Power Control

The 68HC05 controls the Macintosh IIvx power supply through the power fail warning (/PFW) signal. While the computer is turned off, the 68HC05 continually polls the keyboard power button. When this button is pressed, the 68HC05 raises the /PFW signal, causing the power supply to turn on.

The power off function is controlled by software. The "Shutdown" menu command sends a special ADB command to the 68HC05. The 68HC05 responds by pulling the /PFW signal low, causing the power supply to turn itself off.

Power-On Reset

When the 68HC05 microcontroller turns the power supply on, it also asserts the /RESET signal. The /RESET signal, which goes to the processor and other I/O devices, allows the processor to stabilize before executing any cycles.

Accelerator Slot

The Macintosh IIvx includes a slot specifically designed for accelerator cards. An accelerator card contains a faster microprocessor for increased performance.

IMPORTANT
This slot is intended only for accelerator cards. Other types of cards must use the NuBus interface. ▲

Electrical Description of the Accelerator Slot

The Macintosh IIvx accelerator slot is similar to the cache slot in the Macintosh IIci. The most significant difference is that three of the cache control signals (CACHE, /CENABLE, and /CFLUSH) are not connected. For this reason, cache cards designed for the Macintosh IIci will not work in the Macintosh IIvx accelerator slot. However, it is possible to design a Macintosh IIvx accelerator card that will also work in the Macintosh IIci. Table 1-9 shows the pinout for the accelerator slot.

Table 1-9 Macintosh IIvx accelerator slot pinout

Pin	Row A	Row B	Row C
1	A30	/RESET	R/W
2	/HALT	A29	n.c. *
3	A31	A25	A28
4	A26	A27	+5V
5	/RMC	A24	n.c. †
6	D31	GND	+5V
7	D30	D29	n.c.
8	D28	D27	GND
9	D26	D25	+5V
10	D24	D23	GND
11	D22	D21	GND
12	D20	D19	/IPL2
13	D18	D17	n.c. ‡
14	D16	+5V	+5V
15	A22	A21	+5V

continued

Table 1-9 Macintosh IIvx accelerator slot pinout (continued)

Pin	Row A	Row B	Row C
16	A20	A19	GND
17	A18	A17	n.c.
18	A16	A15	GND
19	A14	A13	+5V
20	A12	A11	n.c. §
21	A10	GND	GND
22	FC1	A9	+5V
23	A8	/FPU	GND
24	FC2	FC0	/CIOUT
25	D15	D14	/IPL1
26	D13	D12	/IPL0
27	D11	D10	/CBREQ
28	D9	D8	D7
29	D6	/BGACK	D5
30	D4	D3	D2
31	D1	D0	+5V
32	/ROMOE	A7	A6
33	A5	A4	A3
34	A2	A1	A0
35	/BG	+5V	/CBACK
36	A23	CPUDIS	/BR
37	/DSACK0	/AS	/DS
38	CLK16M	/DSACK1	/BERR
39	GND	+5V	SIZ1
40	GND	n.c. ¶	SIZ0

* Pin C2 was connected to the /STERM signal in the Macintosh IIci cache slot. Pulled up with a 1 KΩ resistor in the Macintosh IIvx.
† Pin C5 was connected to the /CFLUSH signal in the Macintosh IIci cache slot. Pulled up with a 1 KΩ resistor in the Macintosh IIvx.
‡ Pin C13 was connected to the /CENABLE signal in the Macintosh IIci cache slot. Pulled down with a 100 Ω resistor in the Macintosh IIvx.
§ Pin C20 was not connected in the Macintosh IIci cache slot. Pulled down with a 100 Ω resistor in the Macintosh IIvx.
¶ Pin B40 was connected to the CACHE signal in the Macintosh IIci cache slot. Not connected in the Macintosh IIvx.

Since most of the accelerator slot signals connect to MOS (metal oxide semiconductor) devices, the DC load on the processor bus signals is minimal. Only one LS (low-power Shottky) load is connected to the high 16 data lines (D16 to D31). All of the signals can drive at least one TTL (transistor-transistor logic) load (1.6 mA sink current and 400 µA source current).

Table 1-10 lists the descriptions of the accelerator slot signals. Most of the signals are tied directly to the corresponding signals on the 68030 processor bus. Refer to the Motorola *MC68030 Enhanced 32-Bit Microprocessor User's Manual* for a complete description of these signals.

Table 1-10 Accelerator slot signal descriptions

Signal name	Description
A(0–31)	Address lines
/AS	Address strobe
/BERR	Bus error
/BG	Bus grant
/BGACK	Bus grant acknowledge
/BR	Bus request
/CBACK	Cache burst acknowledge
/CBREQ	Cache burst request
/CIOUT	Cache inhibit out
CLK16M	15.6672 MHz clock synchronized to the VASP memory controller
CPUDIS	Disables the CPU and FPU on the main logic board
D(0–31)	Data lines
/DS	Data strobe
/DSACK(0–1)	Data transfer and size acknowledge
FC(0–2)	Function code
/FPU	FPU select signal
/HALT	Halt
/IPL(0–2)	Interrupt priority-level
/RESET	Reset
/RMC	Read-modify-write cycle
/ROMOE	ROM output enable
R/W	Read/write
SIZ(0–1)	Size

Load/Drive Limits for Accelerator Cards

Table 1-11 lists the load presented or drive available for each accelerator slot signal, and indicates whether the signals are inputs or outputs.

In the column labeled *Input/output* in Table 1-11, input refers to a signal from the accelerator card to the main logic board, and corresponds directly to the load shown in the column labeled *Load or drive limits*. Output refers to a signal from the main logic board to the accelerator card, and corresponds directly to the drive shown in that column.

Table 1-11 Load/drive limits for accelerator slot signals

Signal name	Input/output	Load or drive limits
A(0–29)	In/Out	Load: 300 µA/5 mA, 100 pF Drive: 40 µA/.4 mA, 30 pF
A(30–31)	In/Out	Load: 300 µA/8 mA, 100 pF Drive: 40 µA/.4 mA, 30 pF 1 KΩ pull-up
/AS	In/Out	Load: 100 µA/8 mA, 50 pF Drive: 40 µA/.2 mA, 30 pF 1 KΩ pull-up
/BERR	In/Out	Load: 100 µA/8 mA, 50 pF Drive: 40 µA/.4 mA, 30 pF 1 KΩ pull-up
/BG	Output	Drive: 40 µA/.4 mA, 30 pF 1 KΩ pull-up
/BGACK	Input	Load: 100 µA/8 mA, 50 pF 1 KΩ pull-up
/BR	Input	Load: 100 µA/8 mA, 50 pF 1 KΩ pull-up
/CBACK	Input	Load: 100 µA/100 µA, 50 pF 1 KΩ pull-up
/CBREQ	Output	Drive: 40 µA/.4 mA, 30 pF 1 KΩ pull-up
/CIOUT	Output	Drive: 40 µA/.4 mA, 30 pF 1 KΩ pull-up
CLK16M	Output	Drive: 40 µA/.4 mA, 30 pF
CPUDIS	Input	Load: 100 µA/8 mA, 50 pF 1 KΩ pull-down
D(0–23)	In/Out	Load: 300 µA/5 mA, 100 pF Drive: 40 µA/.4 mA, 30 pF
D(24–31)	In/Out	Load: 300 µA/5 mA, 100 pF Drive: 20 µA/.2 mA, 30 pF

continued

Table 1-11 Load/drive limits for accelerator slot signals (continued)

Signal name	Input/output	Load or drive limits
/DS	In/Out	Load: 100 µA/8 mA, 50 pF Drive: 40 µA/.4 mA, 30 pF 1 KΩ pull-up
/DSACK(0–1)	In/Out	Load: 100 µA/8 mA, 50 pF Drive: 40 µA/.2 mA, 30 pF 1 KΩ pull-up
FC(0–2)	In/Out	Load: 100 µA/8 mA, 50 pF Drive: 20 µA/.2 mA, 30 pF 1 KΩ pull-up
/HALT	In/Out	Load: 100 µA/8 mA, 50 pF Drive: 40 µA/.4 mA, 30 pF 1 KΩ pull-up
/IPL(0–2)	In/Out	Load: 100 µA/8 mA, 50 pF Drive: 40 µA/.4 mA, 30 pF 1 KΩ pull-up
/RESET	In/Out	Load: 300 µA/8 mA, 50 pF Drive: 20 µA/.2 mA, 30 pF 1 KΩ pull-up
/RMC	Output	Drive: 40 µA/.4 mA, 30 pF 1 KΩ pull-up
/ROMOE	Output	Drive: 40 µA/.4 mA, 30 pF
R/W	In/Out	Load: 400 µA/8 mA, 50 pF Drive: 40 µA/.4 mA, 30 pF 1 KΩ pull-up
SIZ(0–1)	In/Out	Load: 100 µA/100 µA, 50 pF Drive: 40 µA/.4 mA, 30 pF

Accelerator Slot Power Budget

The power budget for accelerator cards is 5 watts (1 A at +5 volts).

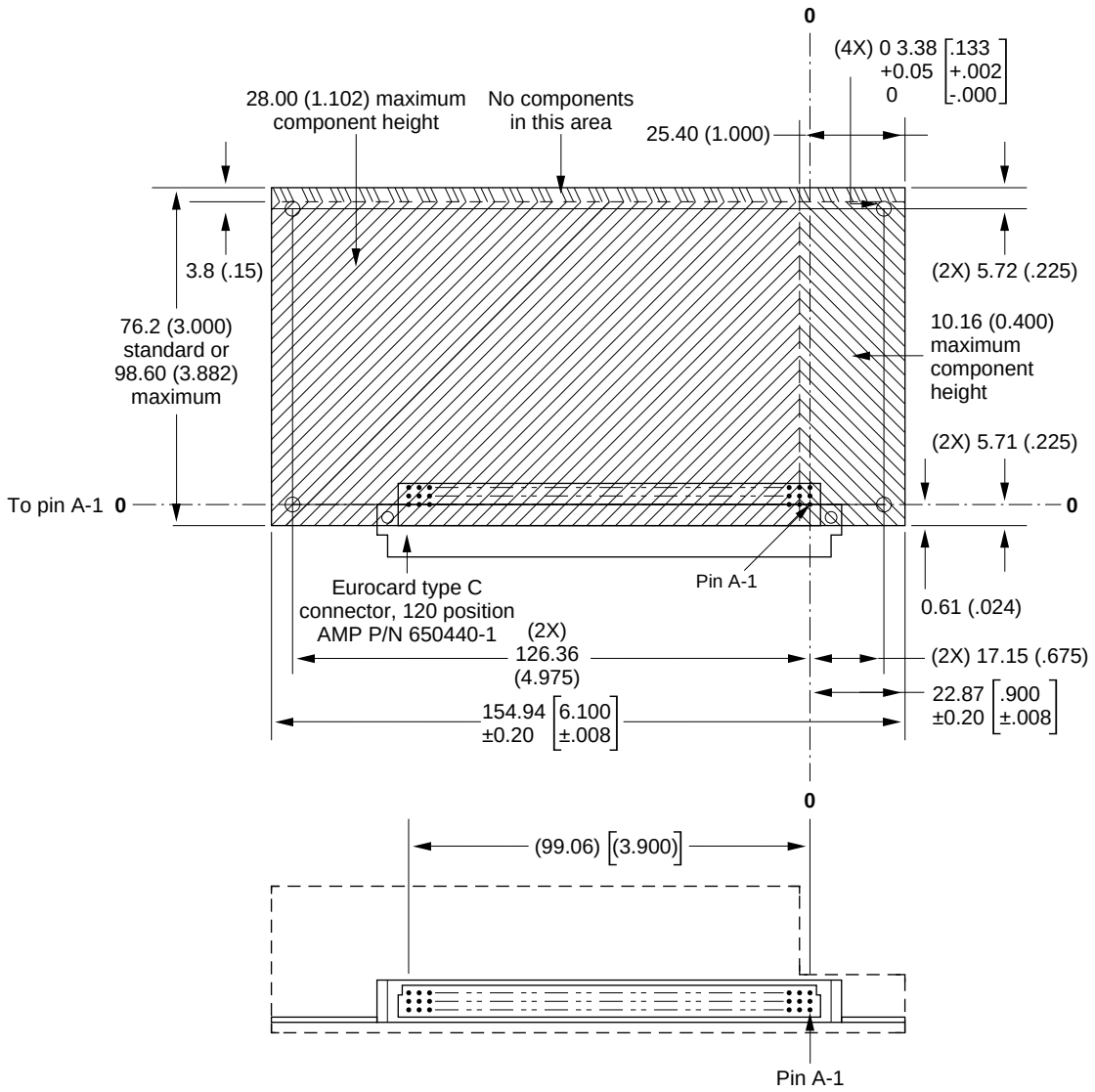
▲ **WARNING**
Cards dissipating more than 5 watts may overheat and damage the Macintosh IIvx computer's circuitry or cause it to become inoperable. ▲

Design Guidelines for Accelerator Cards

Figure 1-5 shows the mechanical design guide for Macintosh IIvx accelerator cards.

Because a properly designed accelerator card can operate in both the Macintosh IIvx and the Macintosh IIci, developers should consider the mechanical and electrical design constraints of the Macintosh IIci cache slot. This information is provided in *Designing Cards and Drivers for the Macintosh Family,* third edition.

Figure 1-5 Macintosh IIvx accelerator card design guide



NuBus Interface

The NuBus expansion interface bus in the Macintosh IIvx is the same design used in the Macintosh IIci. NuBus card electrical specifications and physical design guidelines for the Macintosh IIvx are identical to the Macintosh IIci. Refer to *Designing Cards and Drivers for the Macintosh Family,* third edition, for a complete description of the NuBus expansion interface.

Enclosure Features and Specifications

The Macintosh IIvx computer is housed in a newly designed enclosure measuring 13 inches wide, 16.5 inches deep, and 6 inches high (325 x 412 x 150 mm). The enclosure is constructed of painted sheet metal with plastic front and back bezels. Figures 1-6 and 1-7 show the front and back of the Macintosh IIvx enclosure.

Figure 1-6 Front view of the Macintosh IIvx enclosure

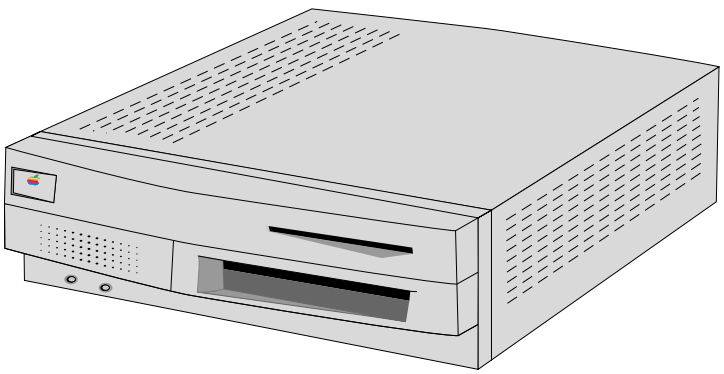
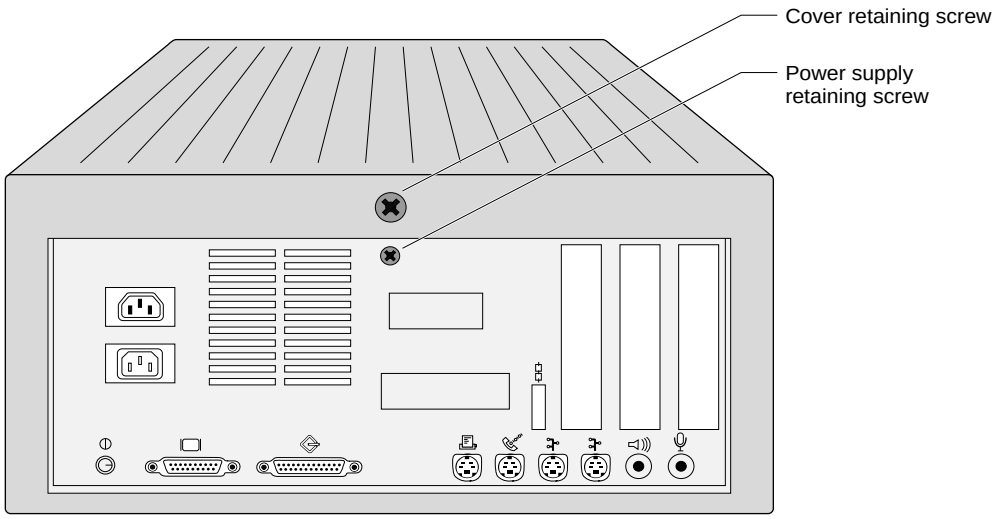


Figure 1-7 Back view of the Macintosh IIvx enclosure



Power Supply

The Macintosh IIvx uses a new power supply. The power supply adapts automatically to the AC voltage applied, from 85 to 270 VAC. The localization package for the computer will include the appropriate power cord for the destination country.

The power supply includes a 3.2-inch (80 mm) fan that provides cooling for the entire system. The power supply also includes a switched convenience receptacle to provide AC line voltage for the monitor. The maximum continuous output current of the convenience receptacle is 3 amps.

Table 1-12 shows the minimum, maximum, and peak ratings for the power supply. The output labeled +5 V TRKL is a trickle supply that is available whenever the computer is plugged in. That output provides power for the 68HC05 microcontroller's real-time clock, parameter RAM, and ADB power-on circuitry. The +12 V output is designed with a peak capacity high enough to meet the combined current demands made by all internal peripheral devices turning on at the same time.

Table 1-12 Power supply ratings

Load	+5 V	+5 V TRKL	+12 V	-12 V	Total power
Minimum	1.5 A	0 A	200 mA	0 A	9.9 W
Maximum	15 A	1 mA	2.5 A	600 mA	112 W
Peak	15 A	1 mA	6 A*	600 mA	130 W*

* For a period of 12 seconds maximum

Internal Mass Storage Devices

The Macintosh IIvx enclosure provides internal mounting locations for one 3.5-inch half-height device and one 5.25-inch half-height device. The 3.5-inch mounting location is intended for a hard disk drive, and provides no external access. The 5.25-inch location is available for optional devices, which slide in from the front after removing the plastic bezel.

Dimensions and Mounting Method for 5.25-inch Devices

Figure 1-8 shows the maximum dimensions for 5.25-inch devices in the Macintosh IIvx. The figure depicts the actual dimensions of the AppleCD 300i CD-ROM drive, which is the largest device the Macintosh IIvx enclosure was designed to accommodate.

Figure 1-9 is a design guide for the mounting rails that secure a 5.25-inch device in the Macintosh IIvx enclosure. These rails are included in the AppleCD 300i mounting kit, which will be available when the Macintosh IIvx is introduced. Developers can purchase mounting rails from Apple or manufacture their own. The Apple Developer Support Center can provide full scale diagrams and plastics specifications for the mounting rails.

Figure 1-8 Maximum dimensions for 5.25-inch devices

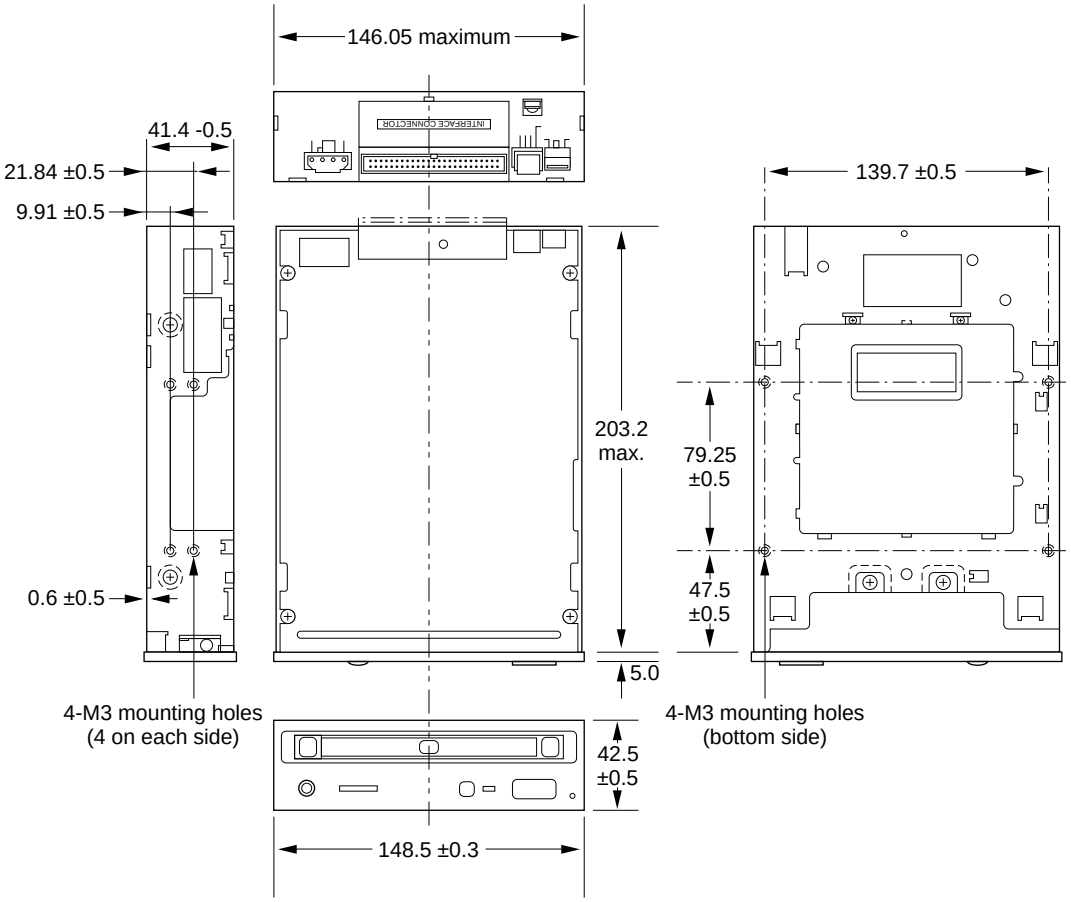
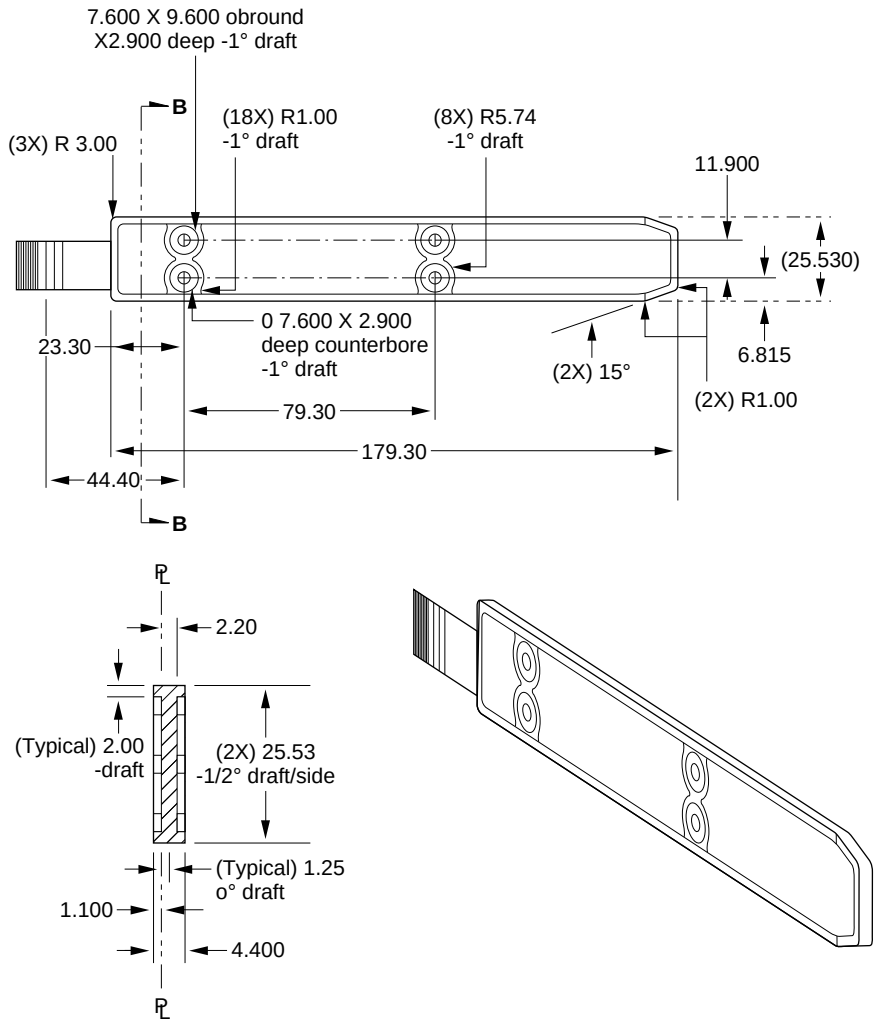


Figure 1-9 Mounting rail for 5.25-inch devices



SCSI Support for Internal Devices

The Macintosh IIvx computer provides two standard power connectors and two 50-pin SCSI connectors for internal devices. The 3.5-inch hard disk must be terminated. The 5.25-inch device must not be terminated.

CD-ROM Bezel

For removable media devices such as CD-ROM, developers must provide a replacement bezel with a cutout for media access. A bezel for the AppleCD 300i is included in the mounting kit for the drive. Developers planning to manufacture their own bezels can obtain full-scale diagrams and plastics specifications from the Apple Developer Support Center.

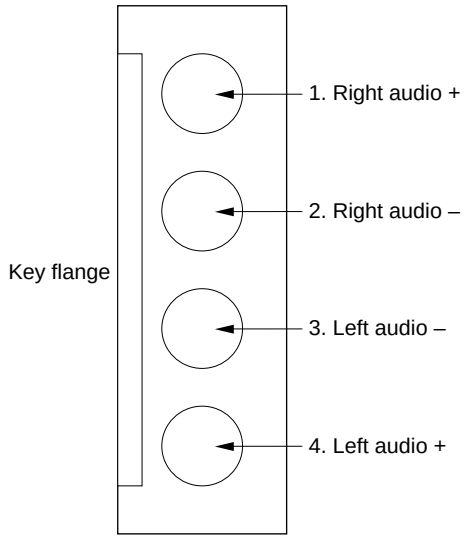
Internal CD-ROM Integration

Some Macintosh IIvx configurations will include the AppleCD 300i CD-ROM drive as standard equipment. See Appendix A, "AppleCD 300i Specifications," for detailed information about this drive.

The internal CD-ROM drive will use SCSI ID number 3. Developers offering internal CD-ROM drives for the Macintosh IIvx should also use SCSI ID number 3.

A CD-ROM audio input connector is provided on the Macintosh IIvx main logic board. The connector is a Molex 22-27-2041-T102 or equivalent. Figure 1-10 shows the connector pinout. The signal level for the input is 0.5 V ± 0.1 V RMS at 47 KΩ.

Figure 1-10 Internal CD-ROM audio connector pinout



Mass Storage Power Budget

Table 1-13 shows the power budget for both the standard 3.5-inch hard disk and an optional 5.25-inch device.

Table 1-13 Power budget for internal mass storage devices

Device	+5 V nominal	+5 V peak	+12 V nominal	+12 V peak
3.5-inch	1 A	1.1 A	800 mA	3 A
5.25-inch	500 mA	500 mA	800 mA	1.5

CHAPTER 2

Software

This chapter summarizes the new software features of the Macintosh IIvx, Macintosh IIvi, and Performa 600 computers, and describes how to use the Gestalt Manager to determine which model your software is running on.

The Macintosh IIvx ROM

This section describes new features of the Macintosh IIvx ROM that are of interest to developers. Most existing applications will work with the Macintosh IIvx computer if they adhere to *Inside Macintosh* guidelines and do not attempt to address the hardware directly.

Memory Manager

The Macintosh IIvx ROM includes enhanced versions of the `LockMemory`, `LockMemoryContiguous`, and `UnLockMemory` routines. These new routines are based on the Macintosh Quadra implementation. When virtual memory is turned off, Macintosh IIvx allocates 8 KB page tables and can individually set each page non-cacheable. When virtual memory is active, page size is 4 KB as with other Macintosh II-family computers.

Because the Macintosh IIvx cache does not snoop, proper use of these Memory Manager calls is critical to correctly setting up shared RAM communication areas. The ability to designate specific blocks as non-cacheable provides support for multiple bus masters without sacrificing the performance improvements of the cache. All Macintosh II-family computers prior to the Macintosh Quadra series guaranteed cache coherency only by disabling the processor data cache.

CD-ROM Booting

Macintosh IIvx includes modifications to allow booting from CD-ROM and similar devices. To boot from CD-ROM, users select the desired CD-ROM volume in the Startup Disk control panel. The system will also search CD-ROM drives and other slow-mounting devices in the normal sequence if a bootable hard disk is not found. As a practical matter, developers should remember that CD-ROM volumes (bootable or not) are ejected before a shut down or restart and therefore may not be available afterward.

The procedure for creating a bootable CD-ROM volume is the same as for any other bootable device. However, because CD-ROM is read-only, some special considerations are required. For example, the desktop files must be properly constructed prior to mastering the disk. Also, the System Folder must contain the appropriate system software as well as the CD-ROM driver software.

The *Apple CD-ROM Handbook* provides useful information about CD-ROM development. For technical information about creating bootable discs, contact the Apple Developer Support Center.

Default Video Mode

The Macintosh IIvx selects 8-bit color mode and a default color desktop pattern when no other video mode is stored in PRAM.

Identifying the Macintosh IIvx

The correct method for software to identify the Macintosh model it is running on is by using the Gestalt Manager routines described in *Inside Macintosh*.

The `gestaltMachineType` identifier for the Macintosh IIvx is 48, the Performa 600 identifier is 45, and the Macintosh IIvi identifier is 44. These values can be used to obtain the machine name string as described in *Inside Macintosh*.

System Software

The Macintosh IIvx is shipped with system software version 7.1. This software provides a number of new features that are documented in the release notes.

System 7.1 introduces a new type of resource file called a **system enabler**. To operate on the Macintosh IIvx and other new machines, a system enabler file must be present in the System Folder. This file contains extensions to the system software necessary to support the new machine. The name of the system enabler file for the Macintosh IIvx is "System Enabler 001." This file must be located at the top level of the System Folder.

Software

AppleCD 300i Specifications

This appendix describes the performance and capabilities of the AppleCD 300i, the internal CD-ROM drive included in some Macintosh IIvx configurations.

General

The AppleCD 300i supports the world-wide standards and specifications for CD-ROM and CD-Digital Audio discs described in the Sony/Phillips Yellow Book and Red Book. The drive can read CD-ROM, CD-ROM XA, CD-I, and PhotoCD discs as well as play standard audio discs.

For improved performance, the AppleCD 300i features a new double-speed mechanism that supports sustained data transfer rates of 300 KB per second—double the transfer rate of previous drives. A 256 KB buffer on the drive controller further enhances performance.

Specifications

Table A-1 lists the specifications and performance characteristics of the AppleCD 300i drive. Table A-2 lists the SCSI commands and messages supported by the drive.

Table A-1 AppleCD 300i specifications

Physical	
Depth (excluding bezel)	203.2 mm (8.00 in.)
Width	146.0 mm (5.75 in.)
Height	41.4 mm (1.63 in.)
Weight	1.25 kg (2.75 lbs.)
General	
Spin up time (maximum)	3 sec (double speed), 2 sec (normal speed)
Spin down time (maximum)	1.5 sec (double speed), 1 sec (normal speed)
Eject time (maximum)	7 sec (double speed), 6.5 sec (normal speed)

continued

Table A-1 AppleCD 300i specifications (continued)

CD-ROM	
Modes supported	CD-ROM (Mode 1 and Mode 2), CD-ROM XA (Mode 2, Form 1 and Form 2), and CD-I (Mode 2, Form 1 and Form 2)
Block lengths supported	
CD-ROM Mode 1	2048, 1024, and 512 bytes
CD-ROM Mode 2	2340, 2336, 1024, and 512 bytes
CD-ROM XA	2647, 2353, and 2336 bytes
Blocks per disc	336,150 (typical)
Data capacity	656 MB, Mode 1 748 MB, Mode 2
Address description	Minutes, seconds, frames
Transfer rate (sustained)	300 KB/sec, Mode 1 (double speed) 150 KB/sec, Mode 1 (normal speed) 342.2 KB/sec, Mode 2 (double speed) 171.1 KB/sec, Mode 2 (normal speed)
Blocks per second	150 (double speed), 75 (normal speed)
Access time (typical)	
Full stroke (first to last block)	520 ms (double speed), 550 ms (normal speed)
Random (block to block)	295 ms (double speed), 350 ms (normal speed)
Track to adjacent track	2 ms
SCSI transfer rate (burst)	1.5 MB/sec, Mode 1 and Mode 2, asynchronous 4 MB/sec, Mode 1 and Mode 2, synchronous
SCSI buffer memory	256 KB
Uncorrected error rate (maximum)	
ECC enabled (Mode 1)	< 1 bit error per 10^{-12} blocks read (double speed) < 1 bit error per 10^{-15} blocks read (normal speed)
ECC disabled (Mode 1 or Mode 2)	< 1 bit error per 10^{-9} blocks read (double speed) < 1 bit error per 10^{-12} blocks read (normal speed)
CD-Audio	
Block lengths supported	2448, 2368, and 2352 bytes
Playing time	74 minutes, 42 seconds
Line output	0.7 volts RMS at 47 KΩ
Headphone output (front panel)	0.65 volts RMS at 32 Ω
Distortion	< 0.04 percent at 1 KHz
Signal to noise ratio	> 80 dB
Frequency response	5 Hz to 20 KHz

Table A-2 AppleCD 300i SCSI implementation summary

Bus phases	Bus free
	Arbitration
	Selection
	Reselection
	Command
	Data
	Status
	Message
Commands	$00, test unit ready
	$01, rezero unit
	$03, request phase
	$08, read
	$0B, seek
	$12, inquiry
	$15, mode select
	$16, reserve
	$17, release
	$1A, mode sense
	$1B, start/stop unit
	$1C, receive diagnostic
	$1D, send diagnostic
	$1E, prevent/allow media removal
	$25, read capacity
	$28, read extended
	$2B, seek extended
	$3B, write buffer
	$3C, read buffer
	$42, read sub-channel
	$43, read TOC
	$44, read header
	$45, play audio
	$47, play audio MSF

continued

Table A-2 AppleCD 300i SCSI implementation summary (continued)

Commands (continued)	$48, play audio track/index
	$4B, pause/resume
	$D8, read CD-Digital Audio
	$D9, read CD-Digital Audio MSF
	$DA, set CD-ROM speed
Status	Status byte = 1 if error condition
	Status byte = 0 if no error
Messages	Command complete
	Disconnect

APPENDIX A

AppleCD 300i Specifications

This Apple manual was written, edited, and composed on a desktop publishing system using Apple Macintosh computers and FrameMaker software. Proof pages were created on an Apple LaserWriter IINTX printer. Final pages were created on the Varityper VT600 imagesetter. Line art was created using Adobe™ Illustrator. PostScript™, the page-description language for the LaserWriter, was developed by Adobe Systems Incorporated.

Text type is Palatino® and display type is Helvetica®. Bullets are ITC Zapf Dingbats®. Some elements, such as program listings, are set in Apple Courier.

WRITER
Mark Turner

EDITOR
Wendy Krafft

ILLUSTRATOR
Sandee Karr

PRODUCTION EDITOR
Gerri Gray